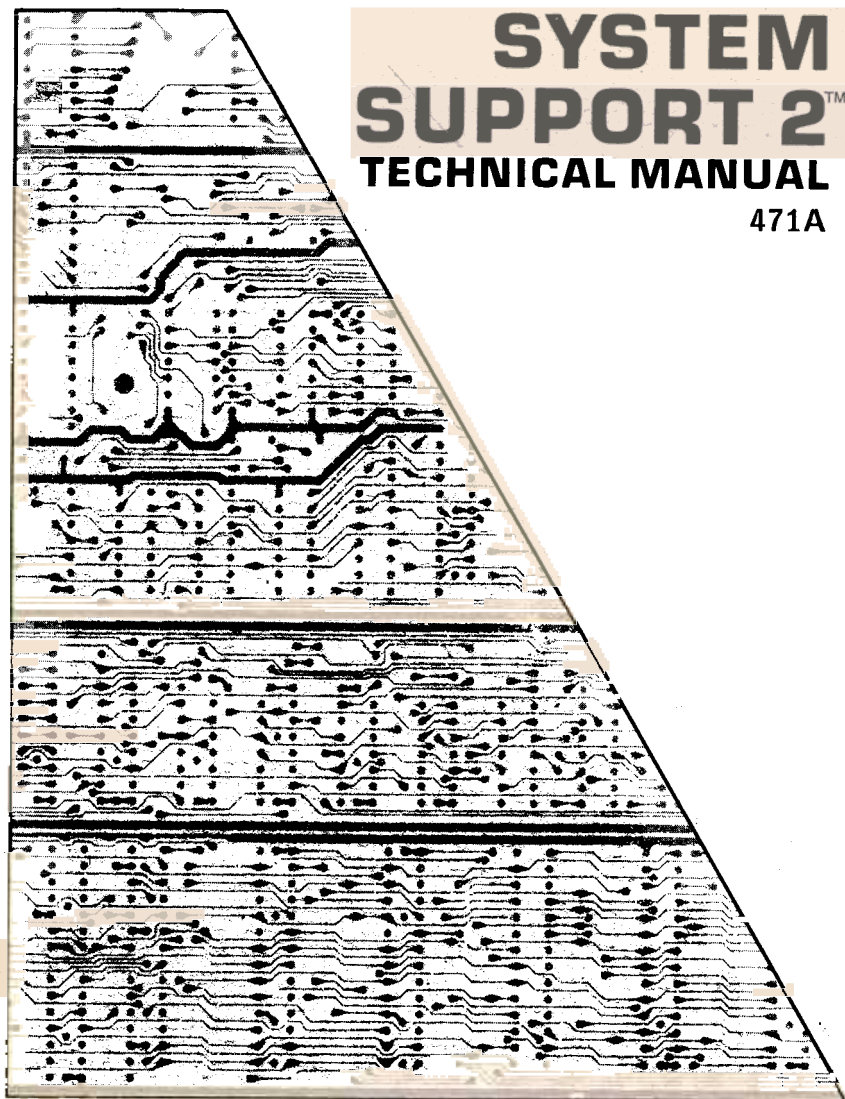


**CompuPro™**

# SYSTEM SUPPORT 2™ TECHNICAL MANUAL

471A



October 1986

**SYSTEM SUPPORT 2™**  
**Technical Manual**

**SYSTEM SUPPORT 2 TECHNICAL MANUAL**  
Copyright 1986 Viasyn Corporation  
Hayward, CA 94545

Part No. 8222-0084A  
Filename: SS2TMMAN

**DISCLAIMER** - Viasyn Corporation makes no representations or warranties with respect to the contents hereof and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, VIASYN reserves the right to revise this publication and to make any changes from time to time in the content hereof without obligation of VIASYN to notify any person of such revision or changes.

**Registered Trademarks:** Centronics; Centronics Data Computer Corp. CompuPro; Viasyn Corporation.

**Compound Trademarks:** Concurrent DOS 8-16; Digital Research Inc. and Viasyn Corporation.

**Trademarks:** The CompuPro logo, System Support 1, System Support 2, CPU-Z, CPU 32016; Viasyn Corporation. Z80; Zilog Corporation.

All rights reserved. No part of this publication may be reproduced or transmitted in any form, or by any means, without the written permission of VIASYN. Printed and assembled in the United States of America.

# Contents

<b>Overall Description</b>	<b>1</b>
<b>Installing the System Support 2 Board</b>	
Basic Installation	2
Switch and Jumper Summary	4
Special Situations	10
<b>Functional Description of Parts</b>	
Interrupt Controllers	11
On-Board Memory	12
Real Time Clock	12
DUART	13
Interval Timers	16
Power Failure Detection Circuit	16
Centronics® Port	16
SCSI Port	19
<b>Programming Considerations</b>	
Interrupt Controllers	22
Enabling Memory Chip Select	24
Real Time Clock/Calendar	24
DUART	30
Interval Timers	32
Centronics Port	33
SCSI Port	35
<b>Appendix A Specifications</b>	<b>40</b>
<b>Appendix B Technical Data Sources</b>	<b>41</b>
<b>Appendix C Schematic Diagram</b>	<b>43</b>
<b>Appendix D Component Layout</b>	<b>52</b>

## LIST OF TABLES

Table 1:	Switch S1 Address Bits	4
Table 2:	Switch S2 and Jumper J11 Settings	5
Table 3:	I/O Port Address Setting	6
Table 4:	I/O Port Map	6
Table 5:	Summary of RAM/ROM Jumper Settings	8
Table 6:	8259A Interrupt Registers	11
Table 7:	RTC Internal Registers	13
Table 8:	DUART I/O Bits	14
Table 9:	Serial Channel Pin-out	15
Table 10:	Centronics Signals	17
Table 11:	Centronics Status Bits	18
Table 12:	Centronics Channel Pin-out	18
Table 13:	SCSI Bus Signals	19
Table 14:	SCSI Status Register	20
Table 15:	SCSI Bus Pin-out	21

## Preface

This manual describes the features and functions of the System Support 2<sup>tm</sup> board. It also contains information on how to program the System Support 2. This is a reference manual for programmers, hardware engineers, and anyone else who needs to understand how the System Support 2 functions in a CompuPro<sup>tm</sup> computer system. It is not a troubleshooting guide or a repair manual.

This manual begins with an overall description of the board and a detailed account of the switch settings for those who are interested in getting "up and running" in a hurry. For those seeking more details on the System Support 2, a functional description follows the switch setting section. Programming considerations, specifications, and schematics are also included.

## Overall Description

CompuPro's System Support 2 is a multifunction board for S-100 computers. Like the System Support 1<sup>tm</sup> board, the System Support 2 combines many small but necessary functions that do not take up enough space to warrant their own board. The System Support 2 meets all the IEEE 696/S-100 specifications and includes the following features:

- Control of eight S-100 vectored interrupts plus seven on-board interrupts.
- Sockets available for up to 64K Static Ram, 128K EPROM, or 16K EEPROM.
- Battery back up for RAM options.
- Battery backed up Real Time Clock.
- Two bi-directional RS-232C serial ports.
- Three Programmable Interval Timers.
- Centronics parallel printer port.
- Small Computer Systems Interface (SCSI) port.
- Supported by CompuPro's Concurrent DOS 8-16<sup>tm</sup> multi-user, multi-tasking operating system.
- Power failure detection.

The separate parts are linked by common Address and Data buses and are orchestrated by common control circuitry.

Further details of the features of the System Support 2 are included in the Functional Description of Parts section of this manual.

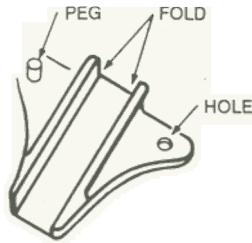
# Installing the System Support 2 Board

## Basic Installation

### Step 1. Unpack the Board.

Along with the board, you will find two card extractors in the plastic bag.

CARD EXTRACTOR



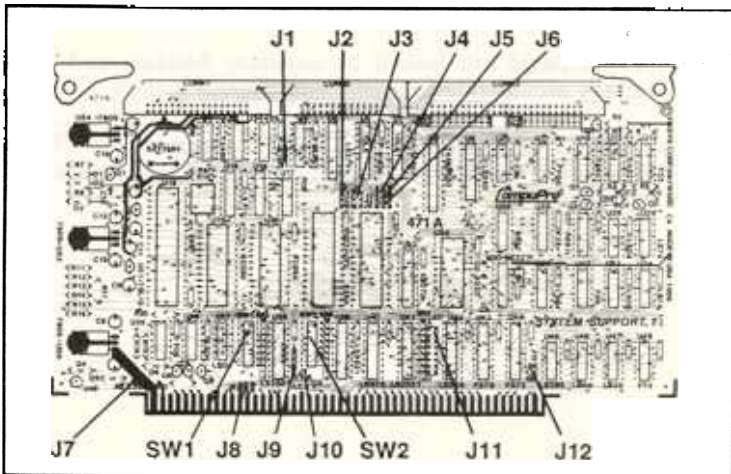
### Step 2. Install the Card Extractors.

Hold the board so the component side is toward you. (See diagram below.)

2. Insert the peg on the card extractor into the hole in the right corner of the board. Fold the extractor over the board's edge until the extractor's hole snaps over the peg.

**NOTE:** Make sure the long edge of the extractor is along the top edge of the board.

3. Repeat for left extractor.





### *Step 3. Check Switch and Jumper Settings*

For standard switch settings for a CompuPro operating system check the operating system Installation Guide. Otherwise, refer to the **Switch and Jumper Summary** in this manual. The locations of the various switches and jumpers on the board are shown in the diagram on the preceding page.

### *Step 4. How to Install Jumper Shunt Connectors*

#### Jumper Shunts

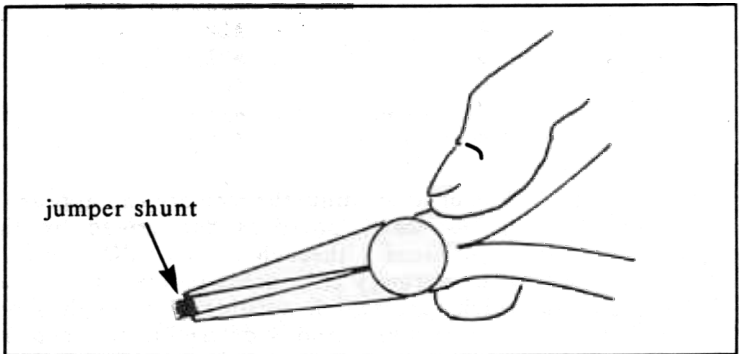
notch



A jumper shunt is a small plastic part used to connect two pins on the jumper connector. Jumper shunts should be installed notch side up.

**IF:** The board is not correctly jumpered.

**THEN:** Use a pair of needle nose pliers to gently remove, and carefully replace the jumper shunt in its proper location.



### *Step 5. Insert the System Support 2 into the S-100 Bus.*

The power to the system must be off. Place the board into a slot towards the back of the enclosure. The edge connector is offset, so the board fits only one way. Push down **GENTLY** until the board is firmly installed.

## Switch and Jumper Summary

This section gives a detailed description of all the switch and jumper settings for the System Support 2. In the following tables a switch setting of "on" corresponds to a binary "0" or "low", and "off" corresponds to a binary "1" or "high".

### Switch S1

Switch S1 is an eight-position dip switch located on the lower left side of the board. Switch paddles 3 through 8 set the memory location of the on-board RAM (or ROM), and each paddle corresponds to a particular address bit as described below. The settings allocate a 256K block of memory space, but the actual amount of memory available will depend on the type and number of memory chips installed. Paddles 1 and 2 on the switch are not used.

Table 1: Switch S1 Address Bits

<u>Switch Position</u>	<u>Address Bit</u>
3	A23
4	A22
5	A21
6	A20
7	A19
8	A18

To CPUs with 24 bits of addressing, the memory can appear in any one of sixty-four 256K pages as determined by the settings of switch positions 3 through 8. To CPUs with 20 bits of addressing, the memory can appear in any one of four 256K pages, in which case switch positions 3 through 6 are set to "on" (0) and positions 7 and 8 determine the memory location.

The two RAM/ROM sockets (U21 and U22) can accommodate memory chips of several sizes. In its standard configuration the board comes with a single 6264 (8K by 8-bit Static RAM). To address this size of RAM, A13 must be set high in software to enable the chip. A17 is used to select between the two RAM/ROM sockets.

With a 6264 in U22, paddles 3-6 "on", and paddles 7 and 8 "off", the memory is at locations C2000h to C3FFFh. If another 6264 is in U21, this memory is at E2000h to E3FFFh.

The other types of memory chips that can be used are described in the on-board memory section this manual.

### Switch S2 (Positions 1 - 4)

Switch S2 is an eight-position dip switch located in the lower left area of the board. Switch positions 1 through 4 set address bits A7 through A4 (see Table 2 below) to determine the base or starting address of the I/O ports on the System Support 2 board. The various possible position 1 - 4 switch settings and their corresponding base addresses are shown in Table 3.

Note: These paddles determine only the high nibble (A7-A4) of the low byte. The low nibble (A3-A0) of the low byte selects which of the 16 ports is addressed. These low nibble bits are addressed in software. The standard CompuPro port map places the 16 I/O ports as shown in Table 4.

Address bits A15 through A8, which determine the upper byte for the hex address, are set by positions A through H of Jumper J11 as shown in Table 2. Normally these bits are hard wired low (ground) by J11. To set the base address above 00F0h, traces on the board must be cut. To do this, carefully cut the trace between the jumper shunt holes of the address bit that you wish to set to "1" or "high".

The standard CompuPro setting for switch S2 positions - 4 places the 16 I/O ports at locations 0050h to 005Fh.

Table 2: Switch S2 and Jumper J11 Settings

<u>Jumper J11</u>		<u>Switch S2</u>	
<u>Position</u>	<u>Address Bit</u>	<u>Position</u>	<u>Address Bit</u>
A	A15	1	A7
B	A14	2	A6
C	A13	3	A5
D	A12	4	A4
E	A11		
F	A10		
G	A9		
H	A8		

With the upper address bits fixed at 00, the following possible base addresses for the ports are:

**Table 3: I/O Port Address Settings**

<u>Switch S2 Position:</u>				<u>Base Address of Ports:</u>
1	2	3	4	
off	off	off	off	00F0h
off	off	off	on	00E0h
off	off	on	off	00D0h
off	off	on	on	00C0h
off	on	off	off	00B0h
off	on	off	on	00A0h
off	on	on	off	0090h
off	on	on	on	0080h
on	off	off	off	0070h
on	off	off	on	0060h
on	off	on	off	0050h
on	off	on	on	0040h
on	on	off	off	0030h
on	on	off	on	0020h
on	on	on	off	0010h
on	on	on	on	0000h

Starting from the base location set by Switch S2, the following port map exists.

**Table 4: I/O Port Map**

Master 8259A (A0=0)	0h
Master 8259A (A0=1)	1h
Slave 8259A (A0=0)	2h
Slave 8259A (A0=1)	3h
Timer/Counter 0	4h
Timer/Counter 1	5h
Timer/Counter 2	6h
Timer/Control	7h
Centronics Command/Status	8h
Centronics Data	9h
Real Time Clock Address	Ah
Real Time Clock Data	Bh
Duart Address	Ch
Duart Data	Dh
SCSI Command/Status	Eh
SCSI Data/Acknowledge	Fh

### *Switch S2 (Positions 5 - 8)*

Switch 2 positions 5 and 6 are connected to the 2681 DUART IP bits 5 and 6, which are user definable input bits (refer to Table 8). Positions 7 and 8 are not used.

### *Jumper J1*

This jumper in the upper left hand side of the board determines which Centronics signal, BUSY\* or ACK\*, will assert an interrupt to the on-board interrupt controllers (8259As). The ACK\* signal is connected via a trace on the board. If BUSY\* is to drive the interrupt, cut the trace on the board between the A and C pins and install a jumper shunt between B and C.

### *Jumpers J2 and J6*

Jumpers J2 and J6 reside in the middle of the board. These jumpers select the signals for the memory options in the RAM/ROM sockets. Chips that can be installed in the sockets are: 6264 (standard), 62256, 2764, 27128, 27256, 27512, 2817A EEPROM, and 2864A EEPROM.

J2 selects a write enable or address bit 14 for the RAM/ROM socket in U21. If a 6264, 62256, 2817A, or 2864A is installed, J2 must be connected from A to C to receive a write enable signal. If a 2764, 27128, 27256, or 27512 is installed, J2 must be connected B to C to receive address bit 14.

J6 selects a write enable or address bit 14 for the RAM/ROM socket in U22. If a 6264, 62256, 2817A, or 2864A is installed, J6 must be connected from B to C to receive a write enable signal. If a 2764, 27128, 27256, or 27512 is installed, J6 must be connected A to C to receive address bit 14.

**NOTE:** To the 2764 and 27128 this is the PGM\* signal that must be set high in software.

### *Jumper J3*

J3 (located in the middle of the board) selects Address bit 14, Address bit 15, or +5V power (or none of these) for the RAM/ROM sockets. J3 is the jumper with three rows of pins. The top row (A) selects +5V for the 2764, 27128, and 27256 memory devices. The bottom row (B) selects Address bit 14 for the 62256 if it is installed. The middle row (C) selects Address bit 15 for the 27512 if it is present. If the 6264, 2817A, or 2864A is installed, NO jumper shunt is installed. Pin 3 of the socket is the RDY/BUSY\* signal of the 2817A which is an output signal. If there is a 2817A installed in U22, then the only chip that can be installed in U21 is another 2817A.

### *Jumpers J4 and J5*

Jumpers J4 and J5 (located in the top middle of the board) determine if the sockets will receive battery backed up power or power from the S-100 bus. J4 controls the power selection for one of the RAM/ROM sockets, and J5 controls the selection for the other socket. With a shunt installed from A to C, the socket will receive battery backed up power. With a shunt installed in the B to C position, the socket will receive power from the +5V supply only. If no chip is installed in the socket, no jumper is required. If there is a ROM or EEPROM installed, use S-100 power (B to C). In the standard configuration, only J5 has a jumper (A to C).

Jumper settings for the RAM/ROM sockets are summarized as follows:

**Table 5: Summary of RAM/ROM Jumper Settings**

JUMPER	6264	62256	2764	27128	27256	27512	2817A	2864A
	A-C	A-C	B-C	B-C	B-C	B-C		A-C
J3	No Shunt	Row B	Row A	Row A	Row A	Row C	No Shunt	No Shunt
J4	A-C	A-C	B-C	B-C	B-C	B-C	B-C	B-C
J5	A-C	A-C	B-C	B-C	B-C	B-C	B-C	B-C
J6	B-C	B-C	A-C	A-C	A-C	A-C		B-C

### *Jumper J7*

This jumper (located on the bottom left side) determines the resistor ladder used in the power failure detection circuitry. On boards that do not have regulators on them, position a jumper shunt from B to C to detect voltage drops from the regulated +5V power supply. On boards that have regulators on them, position a jumper shunt from A to C to detect voltage drops from the unregulated +8V power supply.

### *Jumper J8*

Jumper J8 (located on the bottom left side) selects which S-100 signal, PWRFAIL\* or NMI\*, will be asserted on to the S-100 bus by the System Support 2 in power failure situations. The jumper is hard wired on the board to PWRFAIL\*. To use NMI\*, cut the trace between B and C on the jumper and install a shunt between A and C.

### *Jumper J9*

This jumper (located on the bottom left) offers the option of generating an interrupt to the 8259A interrupt controller when RDY/BUSY\* is driven high by the 2817A EEPROM (if it is installed). In this case, the signal AS is connected to the 8259A by installing a shunt from A to C. NDEF (S-100 pin 66) can also be selected as an interrupt with a shunt installed from B to C. NDEF is user definable and can be used as a vectored interrupt line. Normally no shunt is installed in this jumper.

### *Jumper J10*

The System Support 2 can generate PHANTOM\* when its memory is accessed, or disable itself when another board asserts PHANTOM\*, or do neither. The System Support 2 asserts PHANTOM\* when a jumper is installed from B to C in jumper J10 (located on the bottom left). If a shunt is installed from A to C, the memory on the System Support 2 will be disabled whenever other boards assert PHANTOM\*. Normally there is a shunt from B to C in this jumper.

### *Jumper J11*

See the discussion in the section on Switch 2 for an explanation of this jumper.

## *Jumper J12*

This jumper (located on the bottom right) allows the System Support 2 to power-up with the RAM/ROM sockets activated or inactivated. With a shunt installed from A to C, the RAM/ROM sockets will not respond on power up. With B to C shunted, the RAM/ROM sockets will respond on power up. Normally there is a shunt from A to C in this jumper.

### **Special Situations**

**NOTE:** The System Support 2 will not work with older CompuPro operating systems. Refer to your operating system installation guide to see if the System Support 2 is supported.

CompuPro standard operating systems will only support one System Support board. If you have a System Support 1 board you should remove it from the system before you install the System Support 2.

If you wish to keep a System Support 1 board in the same machine with a System Support 2 (not supported by CompuPro), you will have to set the ports for one of the boards in a location other than 50-5Fh. You will also have to disable the 8259A interrupt controllers on one of the boards. See the System Support 1 technical manual for information on setting the I/O port space on the System Support 1 and for instructions on how to disable the 8259As.

To disable the 8259As on the System Support 2, perform the following steps.

1. Carefully remove the IC in U44. Bend pin 4 of the IC up and away from the chip. Re-install the IC making sure that the bent out pin makes no contact with the socket or any other IC pin.
2. Carefully remove the IC in U47. Bend pin 8 of the IC up and away from the chip. Re-install the IC making sure that the bent out pin makes no contact with the socket or any other IC pin.
3. On the solder side of the board, solder a jumper wire between U44 pin 4 and U44 pin 1 (which is grounded).



# Functional Description of Parts

## Interrupt Controllers

The System Support 2 uses two 8259A chips (one master, one slave) as interrupt controllers. These chips control and prioritize the eight vectored interrupts from the S-100 bus plus seven on-board interrupts. Any (or all) of the interrupts may be masked. The 8259A accepts commands from and releases information to 8085 and 8086 type CPUs. It will not support Z80<sup>tm</sup> type CPUs.

The 8259s are addressed through relative ports 00-03 (50 - 53H standard). Interrupts that are controlled by these chips are the eight vectored interrupts of the S-100 bus, plus interrupts from the 8253 interval timer, the Centronics port, the SCSI port, and the DUART on the board. Jumper 9 allows the selection of an interrupt from the RAM/ROM socket when an EEPROM is present or an interrupt from the S-100 NDEF pin 66.

The interrupt lines for the Master and Slave are as follows:

Table 6: 8259A Interrupt Registers

<u>Interrupt Register</u>		<u>Interrupt Signal</u>
	Master:	
IR0		VI 0 (S-100)
IR1		VI 1 (S-100)
IR2		VI 2 (S-100)
IR3		VI 3 (S-100)
IR4		VI 4 (S-100)
IR5		VI 5 (S-100)
IR6		VI 6 (S-100)
IR7		Slave 8259A
	Slave:	
IR0		VI 7 (S-100)
IR1		Interval Timer 0
IR2		Interval Timer 1
IR3		Interval Timer 2
IR4		Centronics ACK* or BUSY*
IR5		SCSI
IR6		DUART
IR7		EEPROM or NDEF

For more details, see Appendix B for information on how to obtain a data sheet and application notes on the 8259A.

### **On-Board Memory**

Two sockets reside on the System Support 2 for RAM or ROM with 8-bit data bus access. The sockets will accept several chips, but the System Support 2 comes standard with one 6264 Static RAM. Some other chips that can be put in these sockets are: 62256 (32K by 8-bit Static RAM), 2764 (8K by 8-bit EPROM), 27128 (16K by 8-bit EPROM), 27256 (32K by 8-bit EPROM), 27512 (64K by 8-bit EPROM), 2817A (2K by 8-bit EEPROM), and the 2864A (8K by 8-bit EEPROM). The RAM/ROM chips in U21 and U22 are in the lower 28 pins of a 32-pin footprint. The 32-pin footprint can be used in the future to accommodate pin-compatible one megabit EPROM's.

With the 2817A in place, pin 3 is the output signal RDY/BUSY\*. Be sure no shunt is in J3 if a 2817A is present. This signal can be used to generate an interrupt at the 8259A by installing a shunt from A to C in jumper J9.

Battery backup power is available through Jumpers J4 and J5 for RAM chips. See the Jumper setting section of this manual for more information on jumper settings for the RAM/ROM sockets.

### **Real Time Clock/Calendar**

The System Support 2 has a complete time-of-day clock on board that will count seconds, minutes, and hours of the day as well as keep track of the date, day of the week, month and year. The Real Time Clock (RTC) is addressed at relative ports 0A and 0B and has battery backup so that time and date information is not lost when system power is off.

To write to the RTC, the BUSY\* signal must be in the high portion of its cycle. This signal can be monitored through the IP bit 4 of the DUART. If the BUSY\* signal is disasserted, the chip can be written to by first writing to the address port 0A, and then sending the data to the data port 0B. The RTC can be read using the BUSY\* signal as described above, or it can be read without monitoring the BUSY\* signal. To do this, simply write to the address port of the register you wish to read and then read from the data port 0B. The port should be read twice and the results compared in software to determine if the value read is valid.

The internal registers of the RTC are as follows. The address of the register must be sent to the System Support 2 port 0A. There are two registers each for seconds, minutes, hours, days, months, and years. One register is for the one's place and the other is for the ten's place.

**Table 7: RTC Internal Registers**

<u>Register</u>	<u>Address</u>
Seconds (1)	0h
Seconds (10)	1h
Minutes (1)	2h
Minutes (10)	3h
Hour (1)	4h
Hour (10)	5h
Day of the Week	6h
Date (1)	7h
Date (10)	8h
Month (1)	9h
Month (10)	Ah
Year (1)	Bh
Year (10)	Ch

See the programming section of this manual for more information on addressing the RTC. For more details on the 58321 RTC, see Appendix B for information on how to obtain a data sheet.

## **DUART**

A 2681 Dual Asynchronous Receiver/Transmitter (DUART) controls the two serial channels of the System Support 2. The 2681 can be used to control baud rate, word length, parity, and stop bits in RS-232 communications.

The DUART is addressed with relative ports 0C and 0D. Port 0C selects the register in the DUART that is being addressed, and port 0D receives/sends data, commands, and status. There are 16 internal ports on the DUART that can be addressed with port 0C. Data bits D3 to D0 map directly into the A3 to A0 pins on the DUART. The DUART data sheet that explains the addressing of these 16 ports is available on request from Signetics (see Appendix B).

The DUART has eight output bits (OP bits) and seven input bits (IP bits). These bits are defined as follows.

**NOTE:** To set an OP bit low (0), a high (1) has to be written to the set OP register. To set an OP bit high (1), a high (1) has to be written to the reset OP register.

**Table 8: DUART I/O Bits**

	<u>Function</u>
	RTSA - Request to send on channel A of serial port. This output must be set high to allow many terminals to send data.
OP 1	RTSB - Request to send on channel B of serial port. This output must be set high to allow many terminals to send data.
OP 2	RR - Enables the chip select on the RAM/ROM socket. Works in conjunction with jumper J12. The OP bits power up with a high level. If a jumper shunt is installed from B to C, the RAM/ROM sockets will power up with chip select asserted. If a jumper shunt is installed from A to C in J12, the RAM/ROM sockets will power up with the chip selects dis-asserted. The OP 2 bit then has to be set low to enable the RAM/ROM chip select.
	AUTOFD - Centronics printer control signal Auto Feed.
	INIT - Centronics printer control signal Initialize.
	SLCTIN - Centronics printer control signal Select In.
	Not used.
	Not used.
IP 0	CTSA - Clear to send on channel A. Low when terminal is ready to take characters.
	CTSB - Clear to send on channel B. Low when terminal ready to take characters.

**Table 8: DUART I/O Bits**  
(Continued)

<u>Bit</u>	<u>Function</u>
IP 2	DCDA - Data Carrier Detect on channel A. This bit comes from the RS-232 Data Carrier Detect pin 8 channel A. This bit is normally only used when the System Support 2 is DTE.
IP 3	DCDB - Data Carrier Detect on channel B. This bit comes from the RS-232 Data Carrier Detect pin 8 channel B. This bit is normally only used when the System Support 2 is DTE.
IP 4	RTCBSY* - Busy signal from the Real Time Clock. The RTC is busy and must not be written to when this signal is low.
IP 5	User definable as low or high with switch 2 position 5.
IP 6	User definable as low or high with switch 2 position 6.

Signals from the DUART go to a 34-pin edge connector. The signals from DUART A then travel to a DB-25 (D Subminiature) female connector over a ribbon cable. The DUART B signals behave similarly. The pin-out of the two serial channels follows.

**Table 9: Serial Channel Pin-out**

<u>Pin</u>	<u>Signal</u>
2	RXD
3	TXD
5	RTS
7	GND
8	DCD
20	CTS

See Appendix B for information on obtaining RS-232 specifications.

## **Interval Timer**

There is a programmable interval timer (8253) on the board that can be used to generate time delays under software commands. This chip is addressed at relative ports 04-07. The internal registers of the 8253 can be addressed through address bits A0 and A1.

There are three output signals from the 8253 that can generate interrupts to the 8259A interrupt controller. The clock value for the timers is 2 MHz.

See how to obtain the data sheet for the 8253 in Appendix B.

## **Power Failure Detection Circuit**

The System Support 2 includes a circuit that will allow for early detection of power failure in the system. The circuit will assert PWRFAIL\* or NMI\* when either the +8V or +5V signal drops below threshold.

## **Centronics Port**

There is a Centronics parallel interface port on the System Support 2 that can connect directly to Centronics style printers. The Centronics port is addressed at relative ports 08 and 09 and consists of eight data lines plus status and control lines. The output strobe line conforms to the timing specifications of Centronics interface printers.

The printer control signals AUTOFD\*, INIT\*, and SLCT IN\* are controlled by OP bits 3-5 of the 2681 DUART.

An interrupt is generated with the ACK\* pulse when the printer is ready to receive more data. An interrupt can be generated on BUSY\* with Jumper J1. To do this, cut the trace between A and C and install a shunt from B to C on J1.

A summary of the Centronics signals follows. Consult your printer manual for information on how these signals work in your printer.

Table 10: Centronics Signals

<u>Name</u>	<u>Signal</u>
ACK*	Acknowledge - A status signal from the printer that indicates that its operation is complete and it is ready to receive more data.
AUTOFD*	Auto feed - A control signal from the System Support 2 that sets the automatic line feed.
BUSY	Busy - A status signal from the printer that indicates that the printer is busy and is not ready to receive data. This signal is inverted for use on the board.
ERROR*	A status signal from the printer that indicates a printer error.
INIT*	Initialize - A signal sent to the printer from the System Support 2 for initialization.
PE	Paper error - A status signal from the printer that indicates a paper error (e.g. out of paper).
SLCT	Select - A status signal from the printer that indicates that the printer is selected.
SLCTIN*	Select in - A control signal sent to the printer to select it.
STROBE*	Data strobe pulse signal from the System Support 2.

The status bits appear at data bits BD0 - BD4 when relative port 08 is read. The status bits are defined as follows.

**Table 11: Centronics Status Bits**

<u>Data Bit</u>	<u>Signal</u>
D0	BUSY* Printer busy when low
D1	ACK* - Transfer acknowledge low puls
D2	PE - Paper error when high
D3	ERROR* - Printer error when low
D4	SLCT* Printer selected when high

The Centronics signals pass from the System Support 2 to the back panel of the computer over a ribbon cable to a DB-25 (D Subminiature) female connector. The pin-out for the connector is as follows. For more information on the Centronics specifications, see Appendix B.

**Table 12: Centronics Cable Pin-out**

<u>Pin Number</u>	<u>Signal</u>
1	STROBE*
2	Data Bit 0
3	Data Bit 1
4	Data Bit 2
5	Data Bit 3
6	Data Bit 4
7	Data Bit 5
8	Data Bit 6
9	Data Bit 7
10	ACK*
	BUSY
12	PE
13	SLCT
14	AUTOFD*
	ERROR*
16	INIT*
17	SLCTIN*
18-26	Ground



## SCSI Port

The System Support 2 also contains a SCSI port for communications with peripheral I/O devices. This port resides at relative ports 0E and 0F. Data transfers to and from this port go through port 0F. Status from the SCSI port comes in inverted from the SCSI bus through port 0E. SCSI port commands SEL\* and RST\* go out through port 0E.

As defined by the SCSI specification, an initiator in SCSI information transfers is a device that requests the performance of an operation by another SCSI device. The initiator is usually the host system. A target is the device that performs the operation that has been requested by the initiator. The System Support 2 supports a single initiator, non-arbitrating SCSI system and uses the following SCSI signals.

Table 13: SCSI Signals

<u>Name</u>	<u>Signal</u>
-------------	---------------

- |       |                                                                                                                                                                       |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACK*  | Acknowledge - An initiator (System Support 2) driven signal that indicates an acknowledge for a REQ/ACK data transfer handshake.                                      |
| BSY*  | Busy - A status signal from the target that indicates that the SCSI bus is in use.                                                                                    |
| C*/D  | Control/Data - A status signal from the target that indicates if the information on the data bus is control information or data. A low indicates control information. |
| DB0-7 | Data bus bit 0 to 7                                                                                                                                                   |
| DI*/O | Data/I/O - A control signal from the target that indicates the direction of the data transfer on the bus with respect to the initiator.                               |
| MSG*  | Message - A status signal that the target drives low during the message phase.                                                                                        |
| REQ*  | Request - A status signal that indicates that a target is requesting a REQ/ACK data transfer handshake.                                                               |

**Table 13: SCSI Signals  
(Continued)**

Signal

**Reset** - A control signal from the System Support 2 that causes a reset condition.

**Select** - A control signal from the System Support 2 that is used to select a target.

The status bits are read through relative port 0E with the data bits as indicated below. These bits are inverted from the SCSI bus signals.

**Table 14: SCSI Status Register**

<u>Data Bit</u>	<u>Signal</u>
D0	BSY - High when SCSI bus is in use
D4	MSG - High when in Message Phase
D5	C/D* - High in Command Phase
D6	DI/O* - High in Data In Phase
D7	REQ - High when target requests data commands

The pin-out for the SCSI bus follows. All signals are connected to a 50-pin edge connector and have pull up resistors and pull down resistors on them as indicated in the SCSI specification.

**Table 15: SCSI Bus Pin-out**

<u>Pin</u>	<u>Signal</u>
2	Data bit 0
4	Data bit 1
6	Data bit 2
8	Data bit 3
10	Data bit 4
12	Data bit 5
14	Data bit 6
16	Data bit 7
36	BSY*
38	ACK*
40	RST*
42	MSG*
44	SEL*
46	C*/D
48	REQ*
50	DI*/O

Odd pins 1 to 49, even pins 18 to 30, and pin 34 are all grounded. Pin 32 is tied to +5V with a pull-up resistor.

More information regarding the SCSI standard may be obtained in Appendix B.

## Programming Considerations

The following software examples are designed to run with the CompuPro standard operating system. If you are programming in some other environment, study the code listings before adapting your code. No representation is made that this is the best way to program the elements of the System Support 2. Rather, the code is written to illuminate the quirks and pitfalls of programming the System Support 2.

### Programming the Interrupt Controllers

The 8259As reside at relative ports 00 to 03. Ports 00 and 01 address the master's ports, and ports 02 and 03 address the slave's. In the first port of each set, the address bit 0 is equal to 0. In the second port, the address bit 0 is equal to 1.

The chips require several control words for initialization. In this example, four initialization control words (ICW's) and two operational control words (OCW's) are sent to the master and to the slave. These words tell the chip how to handle the interrupts. The following code sets up the interrupt controllers with the following features: level triggered, cascade mode, ICW4 needed, IR7 input has a slave, special fully nested mode, non-polled mode.

```
BASE EQU 50H ;Port base address
MPRTA EQU BASE ;master port A (A0=0)
MPRTB EQU BASE+1 ;master port B (A0=1)
SPRTA EQU BASE+2 ;slave port A (A0=0)
SPRTB EQU BASE+3 ;slave port B (A0=1)

MOV AL,1DH ;ICW1 master
OUT MPRTA,AL ;ICW4 needed

MOV AL,40H ;ICW2 master
OUT MPRTB,AL ;address table
;starts at 80H

MOV AL,80H ;ICW3 master
OUT MPRTB,AL ;slave on IR7
```

```

MOV    AL,11H      ;ICW4 master
OUT    MPRTB,AL   ;special fully
                        ;nested mode

MOV    AL,7FH     ;OCW1 master
OUT    MPRTB,AL   ;slave input mask

MOV    AL,08H     ;OCW3 master
OUT    MPRTA,AL   ;non polled mode

MOV    AL,1DH     ;ICW1 slave
OUT    SPRTA,AL   ;ICW4 needed

MOV    AL,48H     ;ICW2 slave
OUT    SPRTB,AL   ;address table
                        ;starts at 48H

MOV    AL,07H     ;ICW3 slave
OUT    SPRTB,AL   ;slave identifier

MOV    AL,11H     ;ICW4 slave
OUT    SPRTB,AL   ;special fully
                        ;nested mode

MOV    AL,0       ;OCW1 slave
OUT    SPRTB,AL   ;enable all interrupts

MOV    AL,080H    ;OCW3
OUT    SPRTA,AL   ;non polled mode

```

on to other code

Sample code fragment to enable an interrupt

```

CLI                ;disable interrupts while
IN    AL,MPRTB    ; modifying mask register
AND   AL,1111110b ;unmask IRO of master
OUT   MPRTB,al
STI

```

Sample interrupt routine

```

VIO_ENT:PUSH    AX
:
Other code can be done here
:
MOV    AL,60H    ;specific end of interrupt
OUT    MPRTB,AL ; for IRO on master
POP    AX
IRET

```

## Enabling the Chip Select to the RAM/ROM Socket

The OP 2 bit of the DUART enables the chip select on the RAM/ROM socket. This bit works in conjunction with jumper J12. The OP bits power up with a high level. If a jumper shunt is installed from B to C, the RAM/ROM sockets will power up with chip select enabled. If a jumper shunt is installed from A to C in J12, the RAM/ROM sockets will power up with the chip selects dis-asserted. The OP 2 bit then has to be set low to enable the RAM/ROM chip select.

In the following example, J12 is assumed to have a shunt from A to C. The chip select to the RAM/ROM socket is then enabled through OP 2. The DUART is at ports 5C and 5D.

```
DUADD    EQU    5C
DUDATA   EQU    5D
MOV      AL,0EH    DUART set command reg
OUT      DUADD,AL
MOV      AL,04H    set OP2=0
OUT      DUDATA,AL
```

Then to disable the chip select, do the following:

```
MOV      AL,0FH    DUART reset command reg
OUT      DUADD,AL
MOV      AL,04H    set OP2=1
OUT      DUDATA,AL
```

## Programming the Real Time Clock

The RTC resides at relative ports 0A and 0B. The 0A port is used to select the internal register of the clock, and the 0B port is the data port. In addition, the RTC uses the IP bit 4 of the DUART which resides at ports 0C (address) and 0D (data). The clock is read and set by accessing its internal registers. To read and write the RTC, follow the guidelines given below.

#### To read the RTC:

1. Write the number of the register to be read to 0Ah.
2. Read 0Bh.
3. Store the results.
4. Read 0Bh again.
5. Compare the data of the two reads.
6. If the data read is the same, the data is valid.
7. If the data read is not the same, read 0Bh again and compare. Data is valid when two readings are the same.

#### To write the RTC:

1. Select the DUART IP register through 0Ch.
2. Read 0Dh.
3. If IP4 is high, continue. If IP4 is low, go back to step 2.
4. Write the address of the clock register to 0Ah.
5. Write the data to be written to 0Bh.
6. Reset the 1 Hz clock by writing 0Dh to 0Ah and 00 to 0Bh.

#### RTC Internal Registers:

<u>Register</u>	<u>Address</u>
Seconds (1)	0h
Seconds (10)	1h
Minutes (1)	2h
Minutes (10)	3h
Hour (1)	4h
Hour (10)	5h
Day of the Week	6h
Date (1)	7h
Date (10)	8h
Month (1)	9h
Month (10)	Ah
Year (1)	Bh
Year (10)	Ch

A sample program follows.

```
; Display and set the clock on the SS2. This program  
; prints out the contents of the clock and then sets  
; the clock to January 1, 1986.
```

```

SS2_BASE EQU 50H ;base address of board
CLOCK_CMD EQU SS2_BASE + 10 ;Clock command port
CLOCK_DATA EQU SS2_BASE + 11 ; " data port

DUART_CMD EQU SS2_BASE + 12
DUART_DATA EQU SS2_BASE + 13

DUART_INPUT EQU 13 the input register of
DUART
HOUR10 EQU 6 24hr flag in this port

CR EQU 'M'-40H
LF EQU 'J'-40H

EXTRN COUT:NEAR
EXTRN PSTRING:NEAR

CSEG

MOV DX,OFFSET HELLO Explain our output
CALL PSTRING

CALL READTIME
CALL PRINTCLOCK ;print the current time

MOV CX,12 ;number of digits to write
MOV BX,OFFSET TIMESTR ;time to set clock to..
MOV AL,0 ;start at the beginning
WRITELOOP: MOV AH,[BX] ;get the data
SUB AH,'0' ;strip ASCII bias
CALL WRITEDIGIT ;send out the digit
INC BX ;go to next input digit
INC AL ; and next output digit
LOOP WRITELOOP ;and repeat

MOV DX,OFFSET TIME_RESET
CALL PSTRING

CALL READTIME
CALL PRINTCLOCK

RETF

```



PrintClock : display the time/date from the SS2 clock

```
INTCLOCK: MOV    CX,6                ;number of digit pairs
          ; to read
          MOV    AL,0                ;start at the beginning
          CALL   PRINTDIGIT         ;print out the next
          CALL   PRINTDIGIT         ; pair of digits
          CMP    AL,12               ;print a hyphen between
          JE     NOHYPHEN           ; pairs of digits
          XCHG   AH,AL
          MOV    AL,'-'
          CALL   COUT
          XCHG   AH,AL
NOHYPHEN  LOOP   PRINTLOOP
          RET
```

Print the clock digit in AL, auto-increment the count

```
PRINTDIGIT: CALL  READDIGIT
            XCHG  AH,AL
            ADD   AL,'0'
            CALL  COUT
            XCHG  AH,AL
            INC   AL
            RET
```

```
; ReadDigit: AL - digit to read.
; Returns AH - contents of specified port
;           Only AX affected
;
```

```
READDIGIT: PUSH  CX ! PUSH  BX
            MOV   CL,AL                ;save our digit number
            MOV   BX,OFFSET ADDR_VAR
            XLAT  BX                    ;find out where the data
            MOV   BL,AL                ; is saved
            XOR   BH,BH
            MOV   AL,TIME_BUFFER1[BX]
            AND   AL,0FH                ;get rid of high order
            ; nibble
            CMP   CL,10                 ;if hour10,
            JNZ   READD_EXIT           ; bits D2 and D3 must go
            AND   AL,3H                 ;mask off the 24hr flags
READD_EXIT: MOV   AH,AL                ;set up our return codes
            MOV   AL,CL
            POP   BX ! POP  CX
            RET
```

```

; ReadTime - Read the SS2 clock data twice to insure we
; do not read during a digit change.
; Results stored in time_buffer1.
;
READTIME:  PUSH AX ! PUSH CX ! PUSH SI ! PUSH DI
READAGAIN: MOV  DI,OFFSET TIME_BUFFER1 ;read it once
           CALL READTSTR
           MOV  DI,OFFSET TIME_BUFFER2 ;read it twice
           CALL READTSTR
           MOV  CX,12 ;if the 12 bytes
           MOV  SI,OFFSET TIME_BUFFER1 ; are not the
           MOV  DI,OFFSET TIME_BUFFER2 ; same, then
           REPE CMPSB
           JNE  READAGAIN ; read it again
           POP DI ! POP SI ! POP CX ! POP AX
           RET

```

```

; ReadTStr: read the time from the SS2, and save the
; string at es:di. No checking for validity of data
; or masking is done.
;

```

```

READTSTR:  MOV  AH,0 ;clock port to read
           MOV  CX,13 ;number of digits to read
READT_LOOP: MOV AL,AH ;tell clock what we want
           OUT  CLOCK_CMD,AL
           IN  AL,CLOCK_DATA ;get the data from clock
           STOSB ;save our input
           INC  AH ;point to next digit
           LOOP READT_LOOP ; and repeat
           RET

```

WriteDigit: AH = digit to be written; AL = digit #  
to be written to.

```

WRITEDIGIT: PUSH CX ! PUSH BX ! PUSH AX
WRITEWAIT:  MOV  AL,DUART_INPUT ;make sure the clock
           OUT  DUART_CMD,AL ; is not busy
           IN  AL,DUART_DATA
           AND  AL,10H ;strip off to just IP4
           JZ  WRITEWAIT ;go back to waiting
           POP AX ! PUSH AX
           MOV  CX,AX ;save our digits
           MOV  BX,OFFSET ADDR_VAR ;where are we
           XLAT BX ; putting this?
           OUT  CLOCK_CMD,AL ;and ask clock for it
           MOV  AH,CH ;find new digit again

```

```

        CMP     CL, HOUR10
        JNZ    WRITED_DONE
        OR     AH, 8H           ;mask in 24-hour flag
WRITED_DONE MOV    AL, AH
        OUT    CLOCK_DATA, AL ; and give it to clock
        MOV    AL, 0DH         ;point to the reset
        OUT    CLOCK_CMD, AL
        OUT    CLOCK_DATA, AL
        POP    AX ! POP BX ! POP CX
        RET

        DSEG

        ORG    100H

        DB     'MMDDYYHHMMSS-'
TIMESTR   DB     '010186000001'

        ; port addresses for:
        ; Month10, Month1, Day10, Day1, Year10, Year1
        ; Hour10, Hour1, Min10, Min1, Sec10, Sec1
ADDR_VAR  DB     10, 9, 8, 7, 12, 11
        DB     5, 4, 3, 2, 1, 0

HELLO     DB     CR, LF, 'System Support 2 Clock'
        DB     ' Demonstration Version 1.2', CR, LF
        DB     CR, LF, 'The time is ', 0
TIME_RESET DB     CR, LF, 'Time reset to ', 0

TIME_BUFFER1 RS    16
TIME_BUFFER2 RS    16

        end

```

## Programming the DUART

The dual serial channels are addressed through relative ports 0C and 0D. To initialize the serial channels, several mode and command words must be written to the DUART. Code that initializes the DUART follows. In this example, the DUART is initialized to send characters at 19200 baud with eight bits per character, two stop bits, and no parity.

;Routine to initialize the serial channels

```
DUADD EQU 5CH ;Duart address port
DUDATA EQU 5DH ;Duart data port
CSEG
ORG 0
INIT: MOV AL,04H ;Send 80 to the ACR reg
      OUT DUADD,AL ;to select BAUD
      MOV AL,80H
      OUT DUDATA,AL

      MOV AL,0EH ;Set OPO To 0
      OUT DUADD,AL ;RTS/CTS on 0
      MOV AL,01H
      OUT DUDATA,AL

      MOV AL,00H ;Send 13 to mode reg A
      OUT DUADD,AL ;8 bit, no parity
      MOV AL,13H
      OUT DUDATA,AL

      MOV AL,00H ;Send 0F to mode reg A
      OUT DUADD,AL ;2 stop bits
      MOV AL,0FH
      OUT DUDATA,AL

      MOV AL,01H ;Send CC to CSRA reg
      OUT DUADD,AL ;19200 BAUD
      MOV AL,0CCH
      OUT DUDATA,AL

      MOV AL,02H ;Send 15 to command reg A
      OUT DUADD,AL ;enable transmitter/Ireceiver
      MOV AL,15H
      OUT DUDATA,AL
```

```

MOV     AL,0EH           ;put OP1 to 0
OUT     DUADD,AL        ;RTS/CTS on bit 1
MOV     AL,02H
OUT     DUDATA,AL

MOV     AL,08H          ;Send 13 to mode reg B
OUT     DUADD,AL        ;8 bit, no parity
MOV     AL,13H
OUT     DUDATA,AL

MOV     AL,08H          ;Send 0F to mode reg B
OUT     DUADD,AL        ;2 stop bits
MOV     AL,0FH
OUT     DUDATA,AL

MOV     AL,09H          ;Send CC to the CSRB reg
OUT     DUADD,AL        ;19200 BAUD
MOV     AL,0CCH
OUT     DUDATA,AL

MOV     AL,0AH          ;Send 15 to command reg B
OUT     DUADD,AL        ;enable transmitter/receiver
MOV     AL,15H
OUT     DUDATA,AL

```

On to the rest of the program -

## Programming the Interval Timers

The 8253 interval timers reside at relative ports 04-07. Port 04 is the data port for the counter 0, port 05 is the data port for the counter 1, and port 06 is the data port for the counter 1. Port 07 is the command port for all of the counters.

To initialize the counters, control words must be sent to each. In the control words, data bits 6 and 7 are used to select the counter. Data bits 4 and 5 determine in what order the data bytes will be read. Bits 1, 2 and 3 select the mode of operation, and data bit 0 sets the counter as binary or BCD (binary coded decimal).

The code that follows will set up the counters to be square wave generators. The maximum count available to the counters is 65536 with the count going down to zero from the loaded count. The clock is set to 2 MHz.

```
CTRL    EQU    57
CNT0    EQU    54
CNT1    EQU    55
CNT2    EQU    56
;
        MOV    AL,3EH    ;command word for counter 0
        OUT    CTRL    ;square wave generator
        MOV    AL,7EH    ;command word for counter 1
        OUT    CTRL    ;square wave generator
        MOV    AL,OBEH   ;command word for counter 2

        MOV    AL,0AH    ;period of square wave 5 msec
        OUT    CNT0,AL   ;send LSB to counter 0
        OUT    CNT0,AL   ;send MSB to counter 0
        OUT    CNT1,AL   ;send LSB to counter 1
        OUT    CNT1,AL   ;send MSB to counter 1
        OUT    CNT2,AL   ;send LSB to counter 2
        OUT    CNT2,AL   ;send MSB to counter 2
```

on to other programming...

## Programming the Centronics Port

The Centronics port resides at relative ports 08 and 09. In addition, there are 3 OP bits from the DUART that are used to send command signals to the printer. The DUART port address is 0C and 0D. The signals AUTOFD, INIT and SLCTIN are controlled by OP3, OP4, and OP5 respectively. These signals are inverted before they are sent to the printer. Port 09 is the Centronics data port. The status register bits at port 08 are as follows.

DATA BIT	SIGNAL
D0	BUSY* - Printer busy when low.
D1	ACK* - Transfer acknowledge low pulse
D2	PE - Paper error when high
D3	ERROR* - Printer error when low
D4	SLCT* - Printer selected when high

A program that initializes the printer and sends a message to the printer follows.

```
;*          Centronics Test Program
;*          This program sends a repeating message
;*          to a printer.
;*
BASE EQU 50H
CESRD EQU BASE+8H
CEDWR EQU BASE+9H
DUADD EQU BASE+0CH
DUDATA EQU BASE+0DH
CSEG
ORG 00H
MOV AL,0EH ;Set up 2681 OP bits
OUT DUADD,AL ;set the bits
MOV AL,38H ;OP3=0, OP4=0, OP5=0
OUT DUDATA,AL ;to send a 0 to AUTOFD and
MOV AL,0FH ; INIT and a 1 to SLCT IN
OUT DUADD,AL ;set OP3=1, OP4=1, OP5=0
MOV AL,18H
OUT DUDATA,AL
MOV AL,0EH ;Set up 2681 OP bits
OUT DUADD,AL
MOV AL,038H ;OP3=1, OP4=1, OP5=1
```

```

    OUT    DUDATA,AL ;to send a 1 to AUTOFD and
    MOV    AL,OFH    ; INIT and a 0 to SLCT IN
    OUT    DUADD,AL  ;set OP3=0, OP4=0, OP5=1
    MOV    AL,20H
    OUT    DUDATA,AL
READ:  MOV    CX,5
      PUSH   CX
      MOV    SI,offset MESSAGE ;Point to message start
      CALL   PMSG          ;Send message to printer
      POP    CX
      LOOP  READ          ;Do read status, write
      MOV    SI,offset CRLF ; data again
      CALL   PMSG
      JMPS   READ
;
PMSG1: PUSH   SI
      CALL   CENTOUT
      POP    SI
PMSG:  LODSB          ;Pick up character
      OR     AL,AL     ;See if end of string
      JNZ   PMSG1     ;Print char if not end
      RET              ;of string

CENTOUT:
      PUSH  AX
CENTW: IN    AL,CESRD ;Bring in status from printer
      AND   AL,1FH    ;Mask off upper 3 bits
      CMP   AL,1BH    ;See if printer ready
      JNE   CENTW    ;If not, check again
      POP   AX
      OUT   CEDWR,AL  ;Send to printer
      RET

      dseg
      ORG   100H
MESSAGE db 'TEST ',0
CRLF    db 0AH,0DH,0

```



## Programming the SCSI Port

The SCSI port resides at relative ports 0E and 0F. Port 0E is the status and command port, and port 0F is the data port.

The status register bits at relative port 0E are as follows.

<u>Data Bit</u>	<u>Signal</u>
D0	BSY - High when SCSI bus is in use
D4	MSG High when in Message Phase
D5	C/D* - High in Command Phase
D6	DI/O* - High in Data in Phase
D7	REQ - High when target requests data or commands

In the following example, the SCSI target (a hard disk) is first reset. The SCSI status register is then checked to determine if the bus is free. When the bus is free, a SEL\* signal is sent to the target, and the status port is then monitored to determine if the target was indeed selected. The status port is then read to check to see if the target is ready to receive command words. When the target is ready, the command words are sent. The status port is monitored again to see if the target is ready to receive data. When the target is ready, the data is sent. The data is then read back in a similar manner and compared to the data that was sent to make sure that the transfer was made correctly.

### Sample program

```
; This is a very simple program that will read and  
; write different data every 64K to absolute sector 0.  
; There is no initialization and very little error  
; checking. This code is intended as a programming  
; sample and may not be the most efficient way to  
; program the SCSI channel.
```

```

SCDATA    EQU    5FH            ;SCSI data port
SCSC      EQU    5EH            ;SCSI status/command port
SASIREAD  EQU    14H           ;SCSI read command value
SASIWRITE EQU    13H           ;SCSI write command value
;
TRUE      EQU    OFFFFH
FALSE    EQU    NOT TRUE

CR        EQU    0AH
LF        EQU    0DH
EOS       EQU    '$'

                CSEG
                ORG    00H
;
;This first section resets the SCSI device
;
INITSC:    MOV     AL,00H        ;Assert rst*
           OUT     SCSC,AL      ;Send it
           MOV     BX,OFF0FH    ;Set up delay
           MOV     CX,28H
DLOOP:    PUSH   AX ! POP AX    ;Delay for SCSI bus
           PUSH   AX ! POP AX
           LOOP   DLOOP
           MOV     AL,02H        ;Disassert rst*
           OUT     SCSC,AL      ;Send it
           MOV     DL,3         ;Set up delay
TDLY:     MOV     CX,-1
AROUND:   PUSH   AX ! POP AX
           PUSH   AX ! POP AX
           LOOP   AROUND
           DEC     DL
           JNZ    TDLY
           PUSH   DS ! POP ES   ;Set up buffer
           CLD
           MOV     DVAR,OFFFFH
SCSILP:   INC     DVAR          ;Bump to next word to test
           MOV     DI,offset TMPBUF ;Point to sector buffer
           MOV     AX,DVAR       ;Pick up data to fill buf
           MOV     CX,1024/2
           REP    STOSW         ;Fill buffer with test data

;This section calls the main routines of the program

           CALL   SELECT        ;Selects the scsi device
           MOV     SI,offset WRCMND ;Point to wt cmd block
           CALL   SENDCMD       ;Sends the write cmd
           MOV     SI,offset TMPBUF
           CALL   DTOUT         ;Send the data
           CALL   STATUS        ;Checks two status words

```

this point the data has been sent

```
MOV    DI,offset TMP2BUF
XOR    AX,AX
MOV    CX,1024/2
REP    STOSW        ;Clear out the sec buffer
CALL   SELECT      ;Reselect the scsi device
MOV    SI,offset RDCMND ;Point to rd cmd block
CALL   SENDCMD     ;Send read command
CLD
MOV    DI,offset TMP2BUF ;Set up data area
CALL   DTIN        ;Bring data to storage
CALL   STATUS       ;Clear the status bytes
```

```
;
;The data is now in storage
MOV    SI,offset TMPBUF ;Point to both buffer
MOV    DI,offset TMP2BUF ; for string compare
MOV    CX,1024/2
REPE  CMPSW        ;Compare the two buffers
;jump to error routine if sectors did not match
JNE    ERROR
MOV    DX,offset OKMSG ;Print msg to show
CALL   PRINT       ;sector read/wrote ok
JMPS  SCSILP      ;jump back to do rd/wt
; over
```

```
;
ERROR: MOV    DX,offset ERRMSG
CALL   PRINT
MOV    CX,0        ;Exit to CP/M
MOV    DX,0
INT    224        ;Go back to cpm
RETF          ;Should never return
```

; GENERAL SCSI utility routines

;This routine checks to see if the SCSI device is not  
;busy, sends SEL\*, sends id code, and disasserts SEL\*

```
;
SELECT: CLD
BSYHI:  IN     AL,SCSC      ;Check is busy=0 on board
        AND    AL,01H      ;Mask off all but d0
        CMP    AL,00H      ;See if it's 0
        JNZ   BSYHI       ;If it's not, try again
        MOV    AL,01H      ;Assert sel*
        OUT   SCDATA,AL    ;Send it
        MOV    AL,03H      ;Send device id
        OUT   SCSC,AL
BSYLO:  IN     AL,SCSC      ;See if busy=1 on board
        AND    AL,01H      ;Mask
        CMP    AL,01       ;See if it's 1
```

```

JNZ   BSYLO           ;If not, try again
MOV   AL,02H         ;Disassert sel*
OUT   SCSC,AL
RET

```

```

;This routine sends a command to the SCSI device
; SI points to command to send
;

```

```

SENDCMD:  CALL  WAITRQ           ;See if req* is asserted
          IN   AL,SCSC
          AND  AL,60H
          CMP  AL,20H           ;See if still in cmd phase
          JNZ  DONE             ;Quit if not in cmd phase
          LODSB                 ;Pick up cmd byte to send
          OUT  SCDATA,AL        ;Send cmd byte to SCSI
          JMPS SENDCMD
DONE:     RET

```

```

;This routine sends the data to the SCSI port
; SI points to data to send
;

```

```

DTOUT:    MOV   DX,SCDATA
DTOUT1:   CALL  WAITRQ
          IN   AL,SCSC         ;See if still in data
          AND  AL,20H          ; phase
          CMP  AL,00H
          JNZ  DTOUTDONE      ;If in data phase, send
          LODSB                 ; more
          OUT  DX,AL
          JMPS DTOUT1
DTOUTDONE: RET                 ;If not stop sending

```

```

;This routine brings the data from the device and
;stores it in memory
; DI points to destination buffer
;

```

```

DTIN:     MOV   DX,SCDATA
DTIN1:    CALL  WAITRQ
          IN   AL,SCSC         ;Still in data phase ?
          AND  AL,20H
          CMP  AL,20H
          JZ   DTINDONE
          IN   AL,DX
          STOSB
          JMPS DTIN1
DTINDONE: RET                 ;No more data, go back
;

```

;This routine brings in the two status words from the  
;device. The words are disregarded. An error routine  
;could be added here.

```
STATUS      IN      AL,SCDATA
            MOV      CL,AL          ;Store in cl
            CALL     WAITRQ
            IN      AL,SCDATA
            RET
```

;This is the routine that waits for the REQ\* to be  
;asserted.

```
WAITRQ:     IN      AL,SCSC
            AND      AL,80H
            CMP      AL,80H
            JNZ      WAITRQ
            RET
```

; General system utility routines  
; Print a message on console  
; DX points to message to print  
;

```
PRINT:      MOV      CL,9
            INT      224
            RET
```

```
            DSEG
            ORG      100H
DVAR        DW      0000
ERRMSG      DB      CR,LF,'ERROR: SECTOR DID
                ' NOT VERIFY',CR,LF,EOS
OKMSG       DB      ' SCSI ',EOS
RDCMND      DB      SASIREAD,0,0,0,0,0
WRCMND      DB      SASIWRITE,0,0,0,0,0
TMPBUF      RB      1024
TMP2BUF     RB      1024
            DB      0
            END
```

## Appendix A

### Specifications

Size:	
Length .	253 millimeters (10 inches)
Depth .	13 millimeters (0.5 inches)
Height .	127 millimeters (5 inches)
Weight	. 371 grams (13 ounces)
Edge Connectors	. 34 Pin Shrouded Right Angle 26 Pin Shrouded Right Angle 50 Pin Shrouded Right Angle
Timing	. . Meets all IEEE 696/S-100 specifications including systems beyond 10 MHz.
Processors .	Compatible with most CompuPro supported CPU boards *
Memory	. . . 8K by 8 bit static RAM (1) standard
S-100 Address Space	. . Occupies 256K byte memory space and 16 I/O ports
S-100 Memory Address	. Switch selectable to any 256K byte page
Standard I/O Address	. . 0050h to 005Fh
Power Consumption	+8V at 1000 mA typical, 1900 mA maximum +/-16V at 600 mA maximum

\* NOTE: The System Support 2 will not support interrupts on the CPU-Z<sup>tm</sup> and CPU 32016<sup>tm</sup>.

## **Appendix B**

### **Technical Data Sources**

The following information is included here to help those who seek more detailed information than is included in this document.

#### **Centronics Specifications**

Centronics Data Computer Corporation  
1 Wall Street  
Hudson, New Hampshire 03051

Tel. (603) 883-0111

#### **DUART SCN 2681**

Signetics Corporation  
811 East Arques Avenue  
P.O. Box 409  
Sunnyvale, California 94086

Tel. (408) 991-2000

#### **Programmable Interrupt Controller 8259A Programmable Interval Timer 8253**

Intel Literature Department  
3065 Bowers Avenue  
Santa Clara, California 95051

Tel. (800) 538-1876  
California: 800 672-1833

#### **RS232C Standard**

Electronic Industries Association  
Engineering Department  
2001 Eye Street N.W.  
Washington D.C. 20006

**Real Time Clock - RTC 58321**

**Epson America, Inc.  
23600 Telo Street  
Torrance, California 90505**

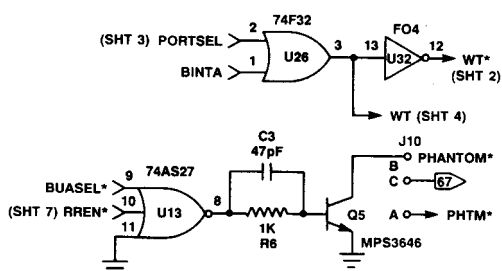
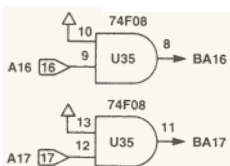
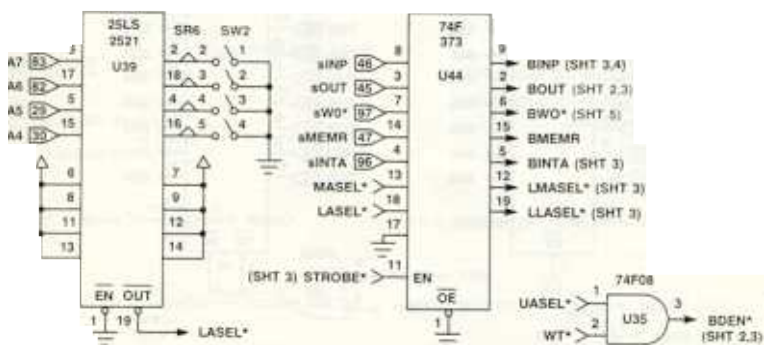
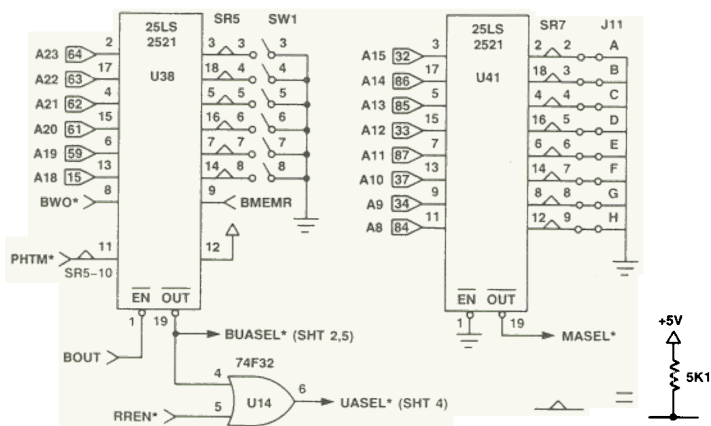
**Tel. (213) 373-9511**

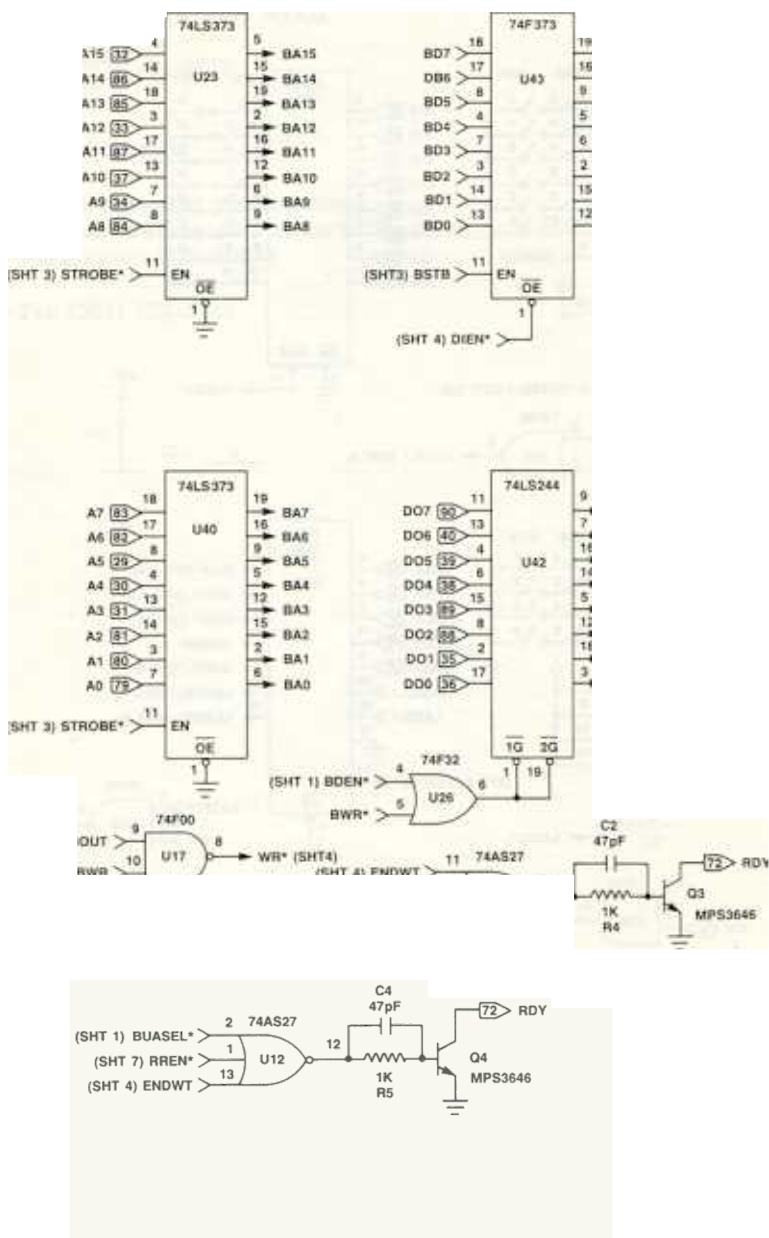
**SCSI Standard**

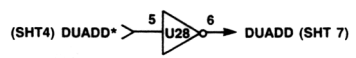
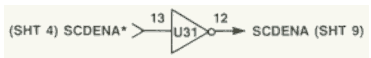
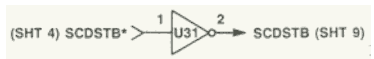
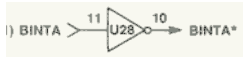
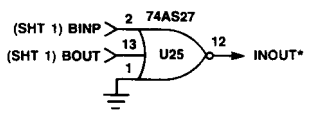
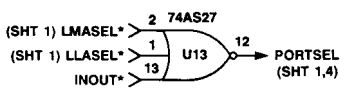
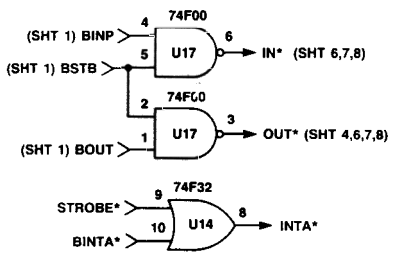
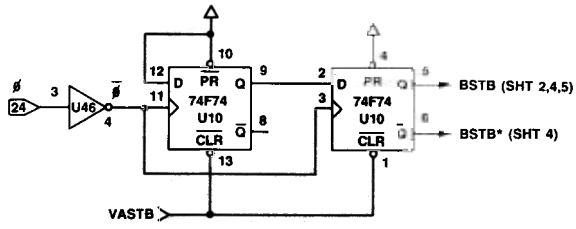
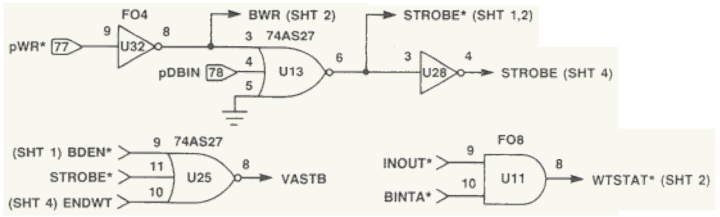
**U.S. Department of Commerce  
National Bureau of Standards/Technology 4-216  
Washington D.C. 20234**

**Tel. (301) 921-3723**

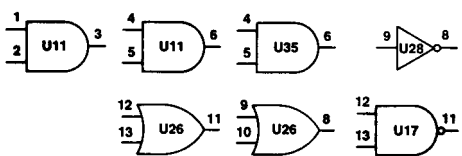


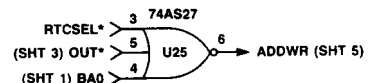
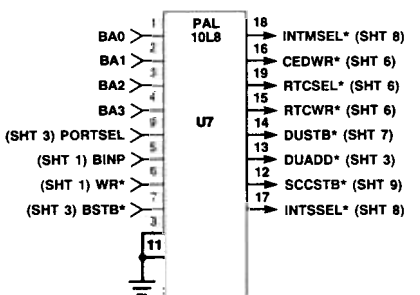
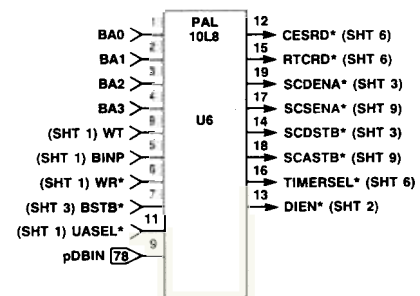
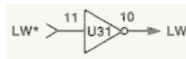
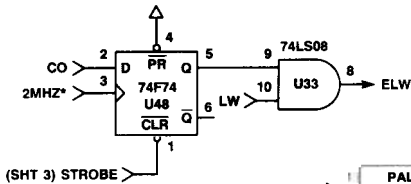
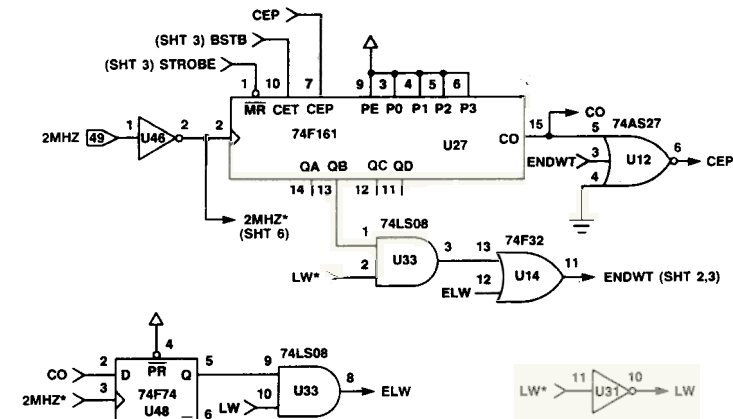


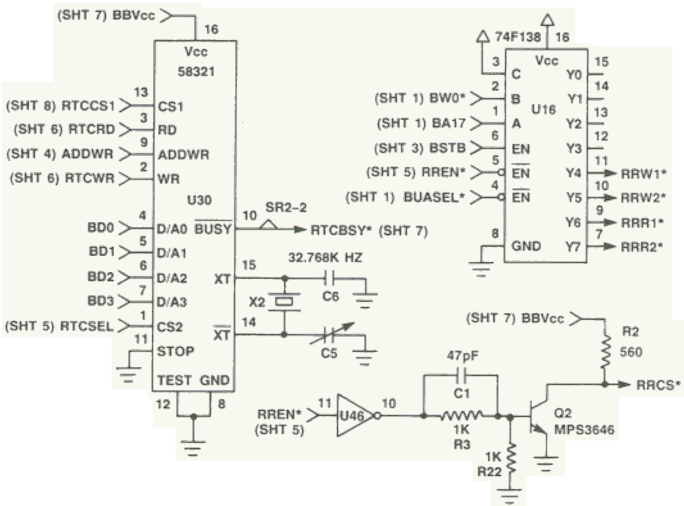
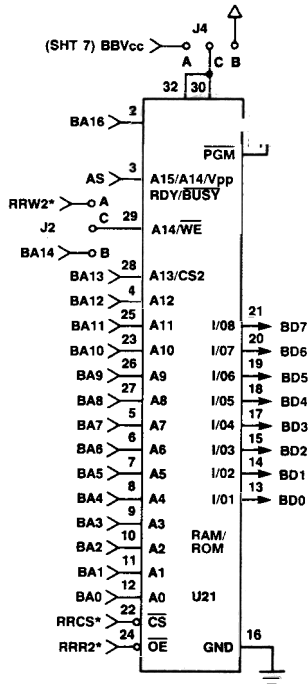
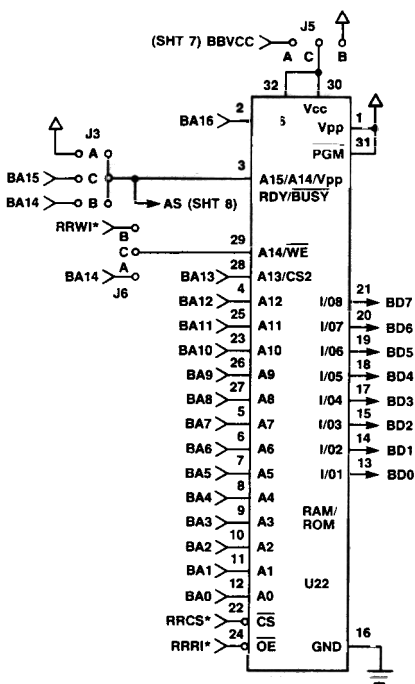


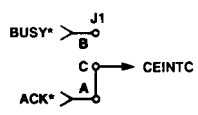
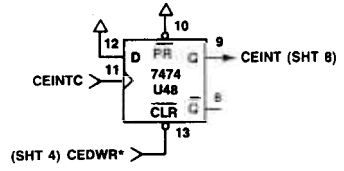
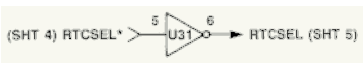
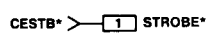
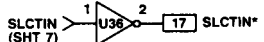
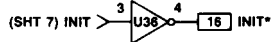
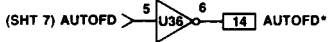
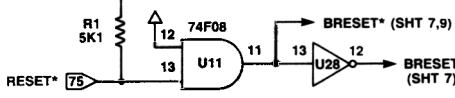
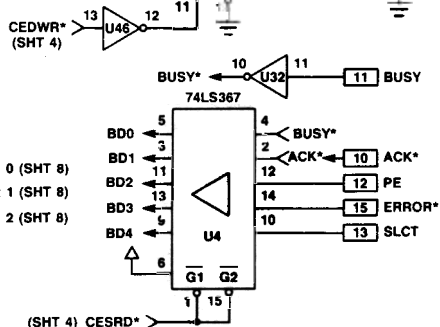
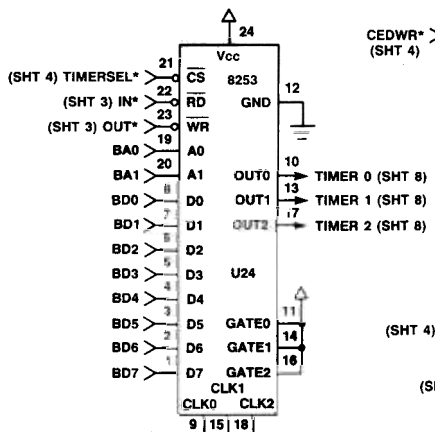
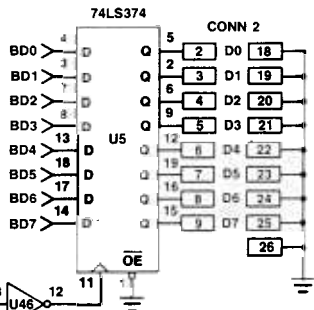
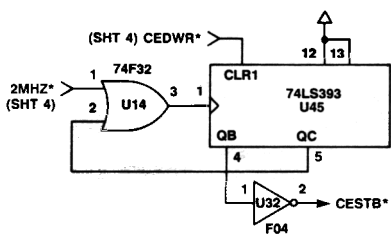


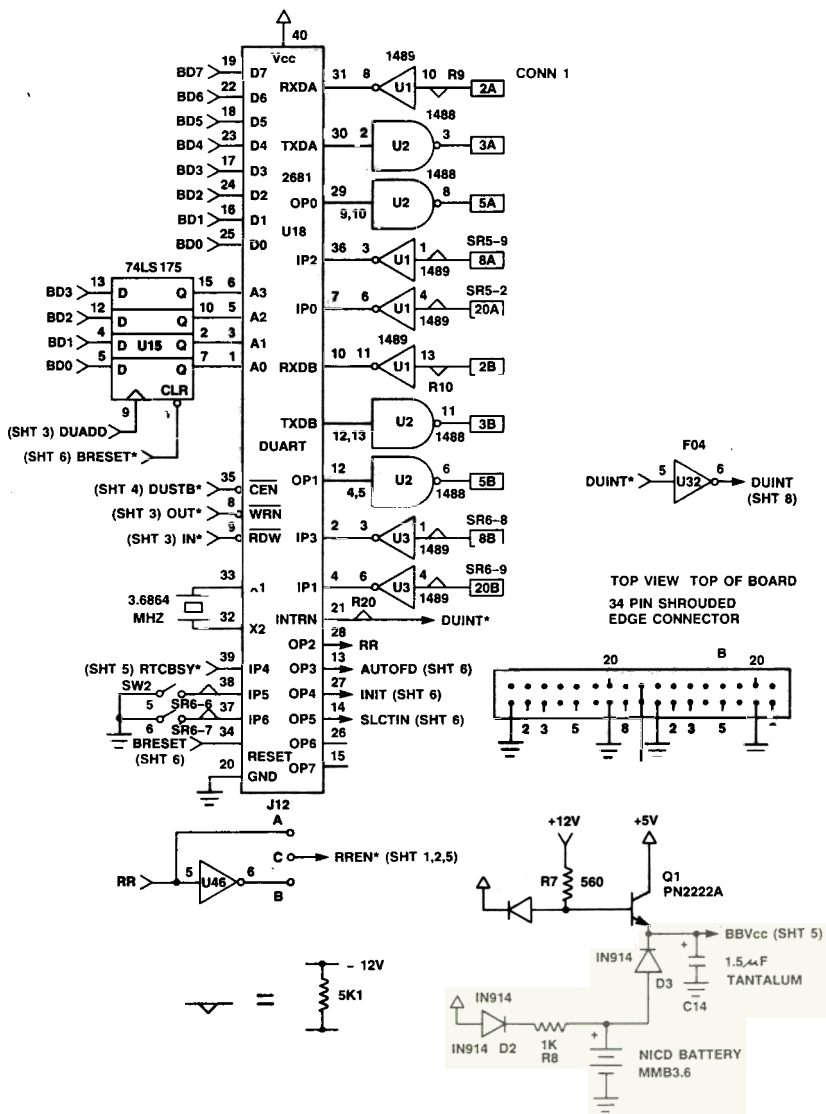
**UNUSED GATES**

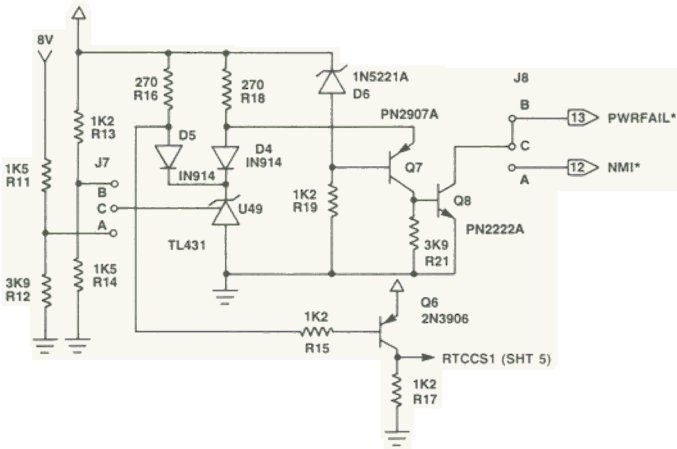
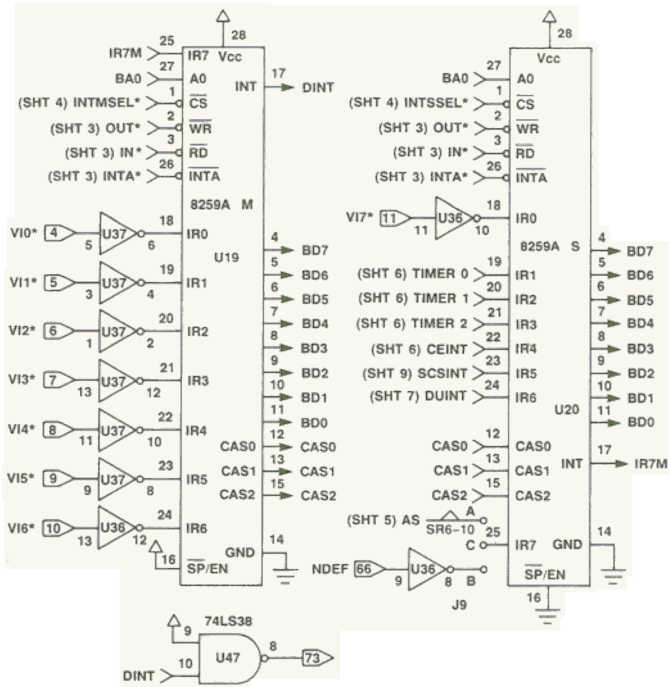




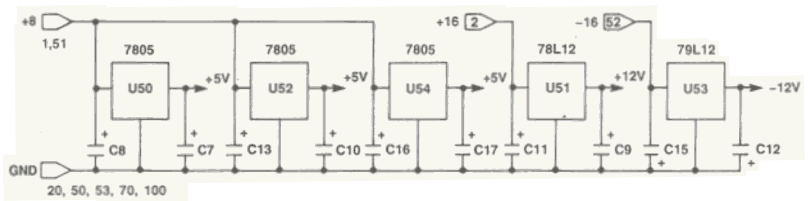
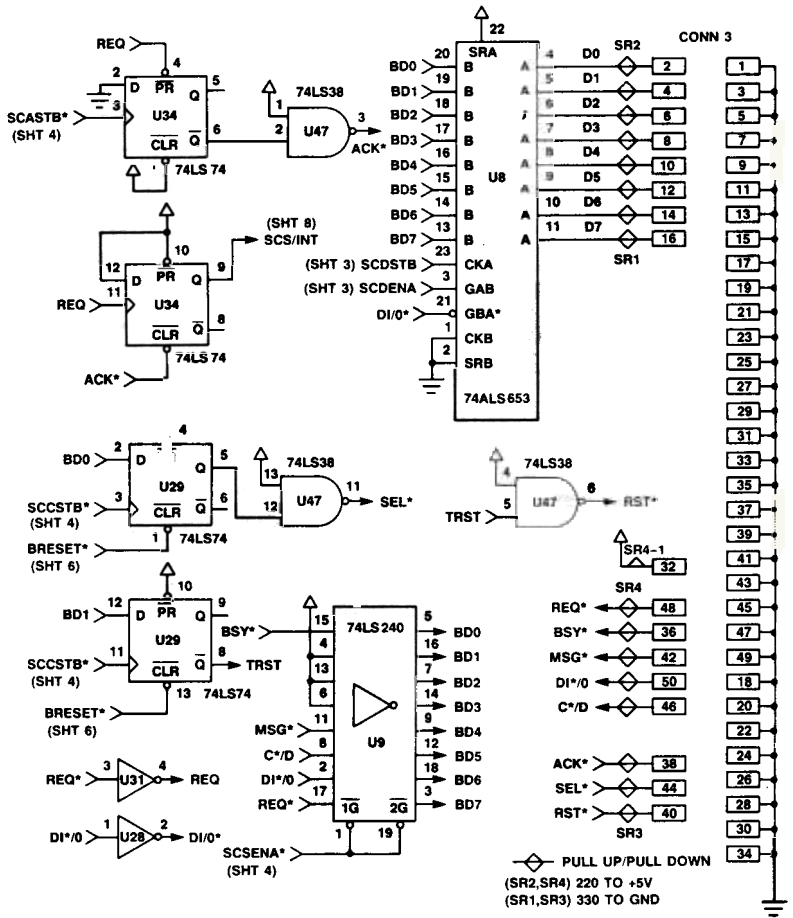


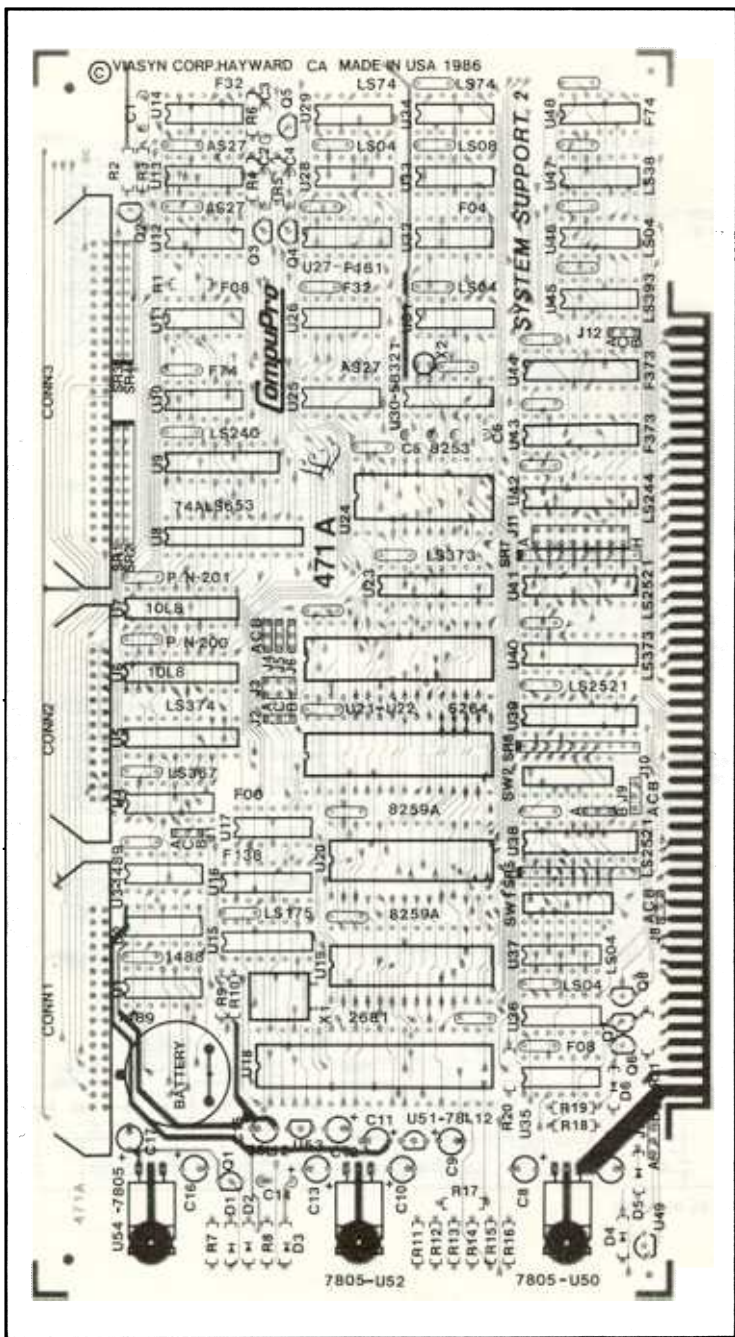












**Component Layout**

## LIMITED WARRANTY

Viasyn Corporation warrants this computer product to be in good working order for a period of ninety days from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, VIASYN will, at its option, repair or replace the item at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of VIASYN. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse or unauthorised modification of the product.

If you need assistance, or suspect an equipment failure, always contact your System Center or dealer first. System Center technicians are trained to provide prompt diagnosis and repair of equipment failures. If you are not satisfied by the actions taken by your System Center or dealer, please call VIASYN at (415) 786-0909 to obtain a Return Material Authorisation (RMA) number, or write to VIASYN at 26538 Danti Court, Hayward, CA, 94545-3999, Attn: RMA. Be sure to include a copy of the original bill of sale to establish a purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location and to use the original shipping container or equivalent. Be sure to mark the RMA number on the outside of the shipping container or delivery may be refused. Contact your System Center/dealer or write to VIASYN at the above address for further information.

All expressed and implied warranties for this product, including the warranties of merchantability and fitness for a particular purpose, are limited in duration to the above listed periods from the date of purchase and no warranties, either expressed or implied will apply after this period.

If this product is not in good working order as warranted above, your sole remedy shall be repair or replacement as provided above. In no event shall VIASYN be liable to you for any damages, including any lost profits, lost savings or other incidental or consequential damages arising out of the use of or inability to use such product, even if VIASYN or a System Center/dealer has been advised of the possibility of such damages, or for any claim by any other party.

If this product is out of warranty, please call or write the VIASYN RMA department to obtain a quotation for factory service. If this product was sold as a system by VIASYN, it may eligible and you may elect to purchase on site/depot maintenance from SPERRY. Contact your System Center/Dealer, your nearest SPERRY office or VIASYN for more details.

If you have purchased a SPERRY service and maintenance agreement, the following two paragraphs also apply:

If VIASYN or its service contractor fails after repeated attempts to perform any of its obligations set forth in this agreement, VIASYN's or its service contractor's entire liability and VIASYN's customer's sole and exclusive remedy for claims related to or arising out of this agreement for any cause and regardless of the form of action, whether in contract or tort, including negligence and strict liability, shall be Viasyn's customer's actual, direct damages such as would be provable in a court of law, but not to exceed the cost of the item of equipment involved.

In no event shall VIASYN or its service contractor be liable for any incidental, indirect, special or consequential damages, including but not limited to loss of use, revenue or profit, even if VIASYN or its service contractor has been advised, knew or should have known of the possibility of such damages; or damages caused by VIASYN's customer's failure to perform its obligations under this agreement; or claims, demands or actions against VIASYN's customer by any other party.

Viasyn Corporation  
26538 Danti Court  
Hayward, CA 94545-3999  
(415) 786-0909  
TWX 510-100-3288

**EFFECTIVE 9/1/86.** This warranty supersedes all previous warranties. All previous editions are obsolete.

9020-0048

---



**Viasyn Corporation**

**26538 Danti Court, Hayward, CA 94545-3999 (415) 786-0909**

\$20.00 82610084A

496100/1