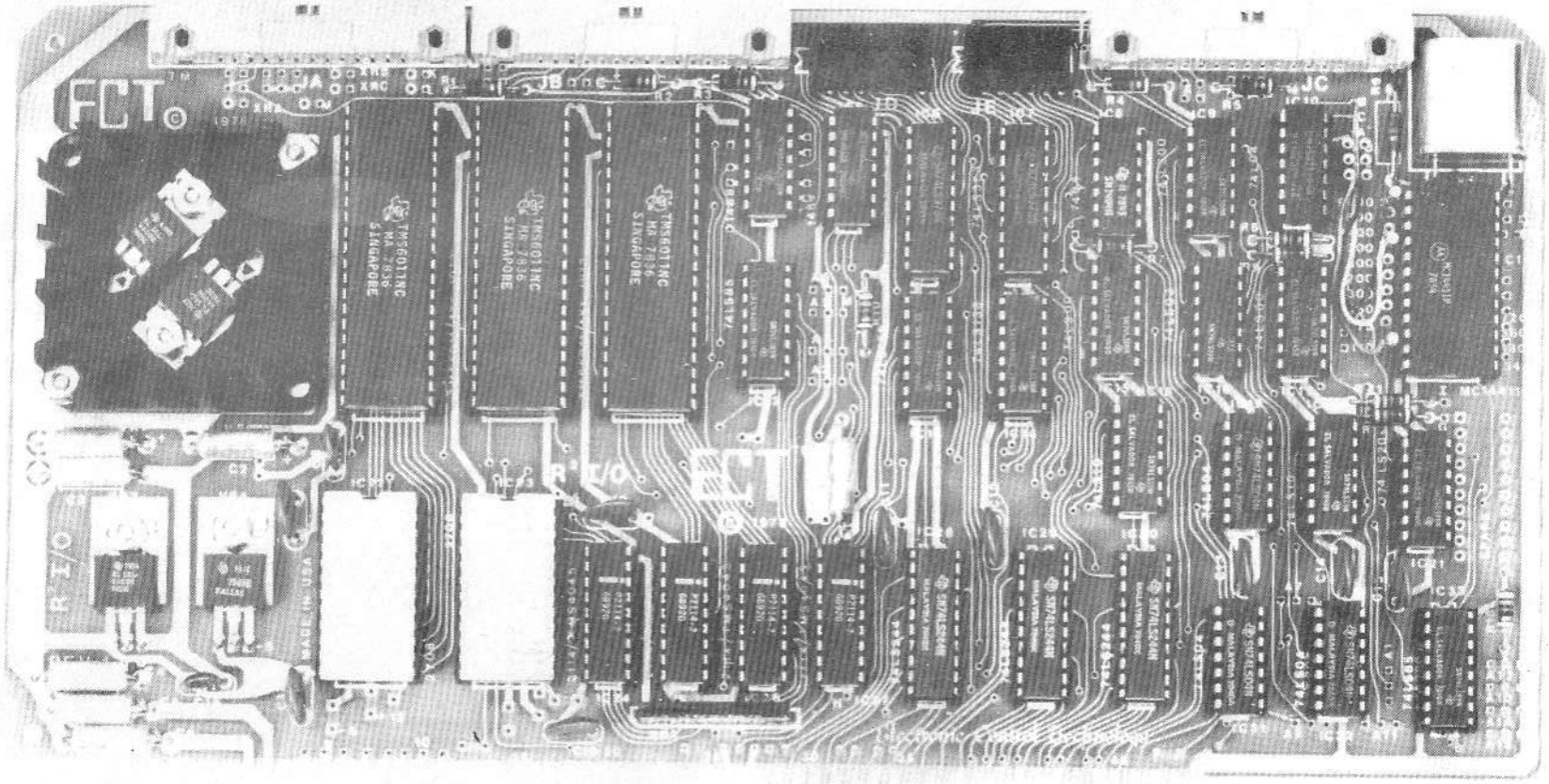
R²I/O



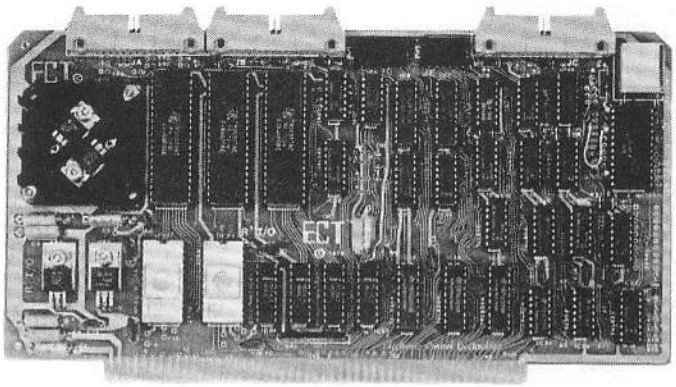
Electronic Control Technology

763 RAMSEY AVE.
HILLSIDE, NEW JERSEY 07205

R²I/O
ROM, RAM & I/O BOARD

ELECTRONIC CONTROL TECHNOLOGY's R²I/O is an S-100 Bus I/0 Board with 3 Serial I/0 Ports, 1 Parallel I/0 Port, 4 Status Ports, 2K of ROM and 2K of RAM. The R²I/0 provides a convenient means of interfacing several I/0 devices, such as - CRT terminals, line printers, modems or other devices, to an S-100 Bus Microcomputer or dedicated controller. It also provides for convenient Microcomputer system control from a terminal keyboard with the 8080 Apple ROM monitor containing executive commands and I/0 routines. Or, it can be used in dedicated control applications to produce a system with a minimum number of boards, since it contains ROM, RAM and I/0.

The standard configuration has the ROM located at F000 with the RAM at F800 and the I/0 occupies the first block of 8 ports. Jumper areas provide flexability to change these locations within reason as well as allow the use of ROM's other than the 2708 — such as the 2716 or similar 24 pin devices. Baud rates are individually selectable in the range of 75 — 9600 and the Voltage levels of the Serial I/0 Ports are RS-232.



- S-100 BUS
- 2K ROM
- 2K RAM
- 3 Serial I/0 Ports
- 1 Parallel I/0 Port
- 4 Status Ports

SPECIFICATIONS

MEMORY (Read/Write): 2K of 2114, 4045 or equal
MEMORY (Read Only): 2K of 2708 or equal (optional 2716, 2308 or similar)
SERIAL I/0 PORTS: 3 UART's TMS6011, AY5-1013A or equal
RS-232 Voltage levels
Baud rates: selectable 75-9600
PARALLEL I/0 PORTS: 1 IN 8 Bit latched
Input loads: 1 low power TTL
1 OUT 8 Bit latched
Output drive: 15 TTL loads
STATUS PORTS: 4 ports — active low Bits 0 & 7
BUS LOADING: 1 low power TTL load per line used
POWER (TYPICAL): +8V @ 600mA
+16V @ 150mA
−16V @ 150mA
SIZE: 5.3" x 10" x 1/16"
PC MATERIAL: G10 or FR4 double sided 2 oz. copper with plated through holes
EDGE CONTACTS: 50 per side on 0.125" spacing, gold over nickel plated
FINISH: Solder mask both sides with silk screened legend
SOCKETS: Low profile sockets for all IC's

Specifications subject to change without notice.

12/78 REV 2/80

8080 APPLE MONITOR COMMAND TABLE

A — Assign I/O
B — Branch to user routine A-Z
C — Undefined
D — Display memory on console in Hex
E — End of file tag for Hex dumps
F — Fill memory with a constant
G — GOTO an address with breakpoints
H — Hex math sum & difference
I — User defined
J — Non-destructive memory test
K — User defined
L — Load a binary format file
M — Move memory area to another address
N — Nulls leader/trailer
O — User defined
P — Put ASCII into memory
Q — Query I/O ports: QI (N)-read I/O; QO(N,V)-send I/O
R — Read a Hex file with checksum
S — Substitute/examine memory in Hex
T — Types the contents of memory in ASCII equivalent
U — Unload memory in Binary format
V — Verify memory block against another memory block
W — Write a checksummed Hex file
X — Examine/modify CPU registers
Y — 'Yes there' find 'N' Bytes in memory
Z — 'Z END' address of last R/W memory location

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ELECTRONIC CONTROL TECHNOLOGY

MEMORY ADDRESSING

The R^2I/O occupies 4K of memory space. The normal ROM address starts at F000 occupies 2K and is immediately followed by 2K of RAM from F800 to FFFF. This 4K memory block can be changed to other 4K boundaries by cutting the appropriate address <A15, A14, A13 & A12> land<s> near IC33 from the plus voltage and jumpering them to ground.

The ROM can occupy the upper 2K while the RAM occupies the lower 2K by cutting the land between the pad connected to IC13 pin 3 from A11 and jumper it to A11.

8080 APPLE MONITOR

The ROM is normally supplied with a monitor 'Apple V1.0 ECT'. The entry point of the monitor is F000, and it will sign on through serial port 'A'.

MEMORY INHIBIT

A logic zero on pad G will inhibit memory, both ROM and RAM and also read and write.

A logic zero on pad I will inhibit the writing to the RAM <protect>.

A logic zero on pad J will inhibit the reading of the entire board <disables the DI bus drivers>.

The phantom pin 67 or similar signal can be used with pad J to selectively disable the read only or with pad G for both read and write.

ROM's

The board is hard wired for 2708's but other 24 pin EPROM's or ROM's can be used. Lands can be cut between each pair of pads connected to pins 18, 19, 20 and 21 to make appropriate changes for the desired EPROM's or ROM's. Check with the data sheet of the desired EPROM's or ROM's for proper connections to these pins. Address A10 is available buffered at pad H. Pins 2 & 5 of IC17 can be cut free and used for additional chip select addressing.

ELECTRONIC CONTROL TECHNOLOGY

I/O PORT ADDRESSING

The board occupies a block of 8 I/O ports. There are three serial I/O ports, one parallel I/O port and four status ports. For serial port 'A', status is on port 0 and data on port 1; for serial port 'B', status is on port 2 and data on port 3; for serial port 'C', status is on port 4 and data on port 5; and for the parallel port, status is on port 6 and data on port 7.

The addressing can be changed in a block of eight ports by cutting the appropriate address <A3, A4, A5, A6 & A7> lands near IC 12 from the plus voltage and connecting them to ground.

Address jumpers A1 & A2 near IC 32 can be used to interchange the serial and parallel I/O ports within the block of eight. Changing both will put the parallel port at port 0 for status and port 1 for data.

STATUS PORTS

Each data port has a status port addressed at the even number port preceeding the data port. Status is active low for Data Available on Bit 0 and Transmitter Buffer Empty on Bit 7. For the serial ports the following errors cause a logic one: Parity Error on Bit 2, Framing Error on Bit 3 and Over-Run on Bit 4.

UART PROGRAMMING

UART pins 35 - 39 program the device. When left open the UART is set up for 8 bits, no parity and 2 stop bits.

Pin 39 is Parity Select - logic one is even parity and logic zero is odd parity

Pins 38 & 37 Word Length Select

WORD LENGTH	38 WLS-1	37 WLS-2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

Pin 36 selects the number of stop bits - a logic one sets up 2 stop bits & a logic zero produces only one.

Pin 35 is parity inhibit - a logic one inhibits the parity bit and a logic zero generates a parity bit between the data bits and the stop bit<s>.

A logic zero or low can be produced on the pins by installing a jumper straight across to the ground pads on the solder side of the board for each UART.

$\overline{\text{Reset}}$, $\overline{\text{POC}}$ & $\overline{\text{EXT CLR}}$ are gated together to reset the UART's. Any or all can be disconnected at IC 18, if required.