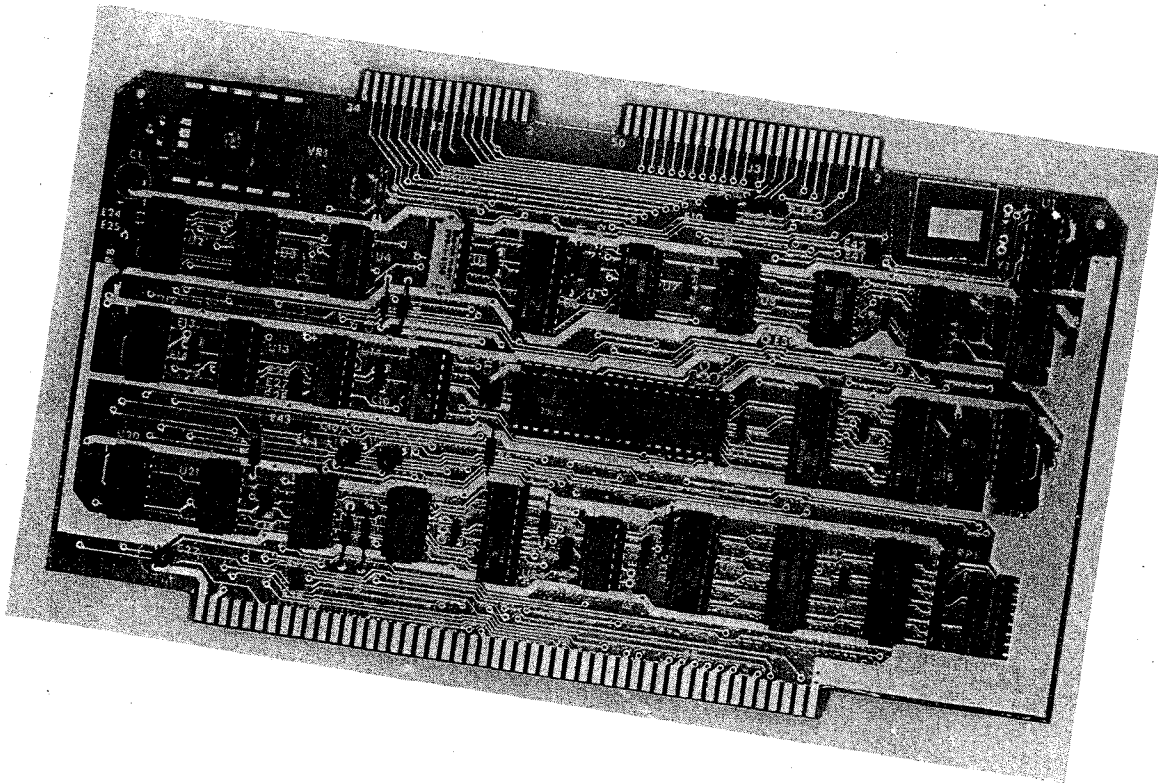


USER'S MANUAL

for the

VERSAFLOPPY™

THE VERSATILE FLOPPY DISK CONTROLLER



S.D. COMPUTER PRODUCTS

P.O. BOX 28810 • DALLAS, TEXAS 75228



S.D. COMPUTER PRODUCTS

P.O. BOX 28810 • DALLAS, TEXAS 75228

STATEMENT OF LIMITED WARRANTY

All components used in this board were purchased through normal OEM sources and any parts which do not function properly will be replaced at no charge for a period of sixty (60) days following the date of shipment.

If this kit does not function properly upon your completion of assembly, it may be returned to S.D. Sales for inspection and evaluation by our Engineering Department.

If the cause of mal or non-function is due to defective parts there will be no charge. If the cause is due to soldering, assembling, etc. of the kit, the charge for inspection, evaluation, and repair will not exceed 10% of the purchase price without your approval. In the event the cost of this service will exceed 10% of sales price S.D. Sales will notify you of the estimated cost before proceeding.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

The assembly of electronic components is essentially the exercise of the art of soldering. If the many connections are soldered properly, the resulting assembly will normally operate properly right from the first application of power. A hasty job here can mean endless hours trying to locate short circuits or intermittent connections. Be sure to read the soldering techniques suggested in Section V before attempting to build this kit.

"Innovations in Digital Applications"

TABLE OF CONTENTS

SECTION	DESCRIPTION	PAGE
1	GENERAL INFORMATION	1
1-1	INTRODUCTION	1
1-2	GENERAL DESCRIPTION	1
1-3	SOFTWARE CONSIDERATIONS	2
2	FUNCTIONAL DESCRIPTION	3
2-1	INTRODUCTION	3
2-2	FD1771B-1	3
2-3	DATA OUT BUS	3
2-4	DATA IN BUS	4
2-5	A0-A7	4
2-6	I/O CONTROL LINES & READ/WRITE CONTROL	4
2-7	WAIT STATE CONTROL AND PRDY	4
2-8	ADDRESS DECODER	4
2-9	DATA IN BUFFER	5
2-10	DATA OUT BUFFER	5
2-11	BI-DIRECTIONAL DATA BUS	5
2-12	INTERRUPT CONTROL & VECTOR GENERATOR	5
2-13	OUTPUT PORT X3 (X = 6 or X=E)	5
2-14	INPUT PORT X3 (X=6 or X=E)	6
2-15	SELECT BUFFER	6
2-16	CONTROL BUFFER	6
2-17	SENSE BUFFER	6
2-18	DATA SEPARATOR	6
2-19	OSCILLATOR	6
3	CONTROL SOFTWARE	9
3-1	INTRODUCTION	9
3-2	SECTOR READ SEQUENCE	9,10,11
3-3	SECTOR WRITE SEQUENCE	11,12,13
3-4	DRIVE SELECTION SEQUENCE	13
3-5	TRACK SEEK AND SIDE SELECT	13,14,15
3-6	"END OF COMMAND" ROUTINE	16,17
4	CONSTRUCTION	18
4-1	INTRODUCTION	18
4-2	ASSEMBLY PROCEDURE	18,19
4-3	VOLTAGE CHECK	20
5	JUMPER OPTION SELECTION/INSTALLATION	21
5-1	INTRODUCTION	21
5-2	I/O PORT ADDRESS SELECTION	21
5-3	CPU SELECTION	21
5-4	INTERRUPT OPTIONS	22
5-5	DRIVE SELECTION	23

TABLE OF CONTENTS

SECTION	DESCRIPTION	PAGE
6	SOFTWARE OPTIONS	24
6-1	INTRODUCTION	24
6-2	CONSOLE PORT ADDRESS AND BIT MASKS	24,25
6-3	DRIVE PARAMETER OPTIONS	25
6-4	CLOCK RATE PARAMETER	25
6-5	BOOTING UP CP/M	26
7	CHECK OUT	27
7-1	INTRODUCTION	27
7-2	OSCILLATOR	27
7-3	RE AND WE PULSES	27
7-4	I/O PORT WRITE/READ VERIFICATION	27,28
7-5	HEAD LOAD MONOSTABLE	28
8	DIAGNOSTIC SOFTWARE	29
8-1	INTRODUCTION	29
8-2	DIAGNOSTIC TEST START-UP	29,30
8-3	DIAGNOSTIC TEST 00 (SEEK TEST)	30
8-4	DIAGNOSTIC TEST 01 (WRITE/READ)	30,31
8-5	DIAGNOSTIC TEST 02 (READ TEST)	31
8-6	DIAGNOSTIC TEST 03 (RANDOM WRITE/READ)	31
8-7	DIAGNOSTIC TEST 04 (MULTI-DRIVE RANDOM WRITE/READ)	31
8-8	DIAGNOSTIC TEST 05 (FORMATING)	31,32
8-9	DIAGNOSTIC TEST 10 (LOAD FROM DISK)	32
8-10	DIAGNOSTIC TEST 11 (SAVE ON DISK)	32,33
8-11	DIAGNOSTIC TEST FF (JUMP)	33
8-12	DIAGNOSTIC ERROR REPORTING	33,34
APPENDICES		
A	VERSAFLOPPY SCHEMATIC DIAGRAM	
B	VERSAFLOPPY PARTS LIST	
C	VERSAFLOPPY PARTS PLACEMENT DRAWING	
D	CONTROL SOFTWARE LISTING	
E	DIAGNOSTIC SOFTWARE LISTING	

SECTION I
GENERAL INFORMATION

1-1 INTRODUCTION

VERSAFLOPPY the versatile floppy disk controller board from S.D. COMPUTER PRODUCTS, provides a low cost means of interfacing to many of the available floppy disk drives, including: Shugart SA400/SA450; Shugart SA800/SA850; MFE 700/750; Persci 70; Persci 277; GSI GS-105. VERSAFLOPPY operates with many 8080 and Z-80 CPU boards on the S-100 Bus. However, VERSAFLOPPY was designed to be used optimally with S.D.'s SBC-100, single board computer, and 32K Expandoram Boards to form a complete, low cost, disk based, computer.

1-2 GENERAL DESCRIPTION

At the heart of VERSAFLOPPY is the powerful Western Digital FD1771B-1 NMOS LSI controller chip. This device performs most of the timing and control functions required by floppy disk drives such as:

1. Head load/unload
2. Track seeking with verification
3. Address mark detection/generation
4. Serial to parallel data conversion during reads
5. Parallel to serial data conversion during writes
6. CRC error code checking/generation
7. IBM 3740 Soft sector compatible recording

During sector reading and writing, the data rate is synchronized with the CPU by inserting wait states until the FD1771B-1 is ready for the next word. On full size drives the data rate is one word (8bits) every 32 microseconds (31,250 words/sec). On mini-drives it is one word (8bits) every 64 microseconds (15,625 words/sec).

1-3 SOFTWARE CONSIDERATIONS

The control function has been designed to be evenly distributed between the hardware circuit and the control software allowing a great deal of flexibility for the user. A version of the control software is supplied with VERSAFLOPPY configured to run on the SBC-100 single board computer. This may be modified to meet the user's specific software interface requirements, such as register usage, parameter hand-offs and data formats.

Also available from S.D. COMPUTER PRODUCTS is a version of CP/M configured to run on the SBC-100, VERSAFLOPPY and 32K Expandoram board combination. This allows using several disk based versions of Fortran and Basic.

SECTION II

FUNCTIONAL DESCRIPTION

2-1 INTRODUCTION

Functionally, VERSAFLOPPY consists of two main parts: hardware, and the software which controls it. The hardware allows the computer to control the drive selection, head loading, track seeks, formatting, reading and writing operations. The software, as described in Section 3, must direct the hardware in each of these operations. The major functions contained in the VERSAFLOPPY hardware are shown in the block diagram. (Fig. 2-1) Table 2-1 lists the S-100 Bus signals used by VERSAFLOPPY.

2-2 FD1771B-1

The FD1771B-1, floppy disk controller chip, performs track to track stepping timing, head load timing, serial to parallel data conversion; parallel to serial data conversion; error code checking/generation, and IBM 3740 softsector compatible recording. After each operation is completed, the chip interrupts the CPU. (option) (For complete description, see Western Digital FD1771B-1 specification). I/O ports X4, X5, X6 and X7 (X=6 or E) are contained within this device.

2-3 DATA OUT BUS

The 8 bit DATA OUT BUS is the S-100 path for transferring data from the computer (CPU) to the output ports on the VERSAFLOPPY board.

2-4 DATA IN BUS

The 8 bit Data In Bus is the S-100 path for transferring data from the input ports on the VERSAFLOPPY board to the computer (CPU). Additionally, the interrupt vector is passed to the CPU on the Data In Bus during the interrupt acknowledge cycle.

2-5 A0-A7

The A0-A7 low order eight address lines are used by the computer (CPU) to select the various input/output ports on the board.

2-6 I/O CONTROL LINES AND READ/WRITE CONTROL

The I/O Control lines consist of $\overline{\text{PWR}}$, PDBIN, SOUT, SINP. These lines are used to control the input and output operations from/to the I/O ports on the board.

2-7 WAIT STATE CONTROL AND PRDY

The Wait State Generator is used by VERSAFLOPPY to delay the input and output operations until the FD1771B-1 chip is ready to transfer a word. This PRDY line puts the CPU in a wait state during the delay. Wait states are only generated during sector reads and writes (which use I/O port X7).

2-8 ADDRESS DECODER

The Address Decoder detects when a port address used on VERSAFLOPPY is present on (A0-A7) the low order eight bits of address from the CPU. The output of the decoder is used to gate read and write pulses to the I/O ports.

2-9 DATA IN BUFFER

The Data In Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY from the S-100 Data in Bus. This buffer is enabled during input port reads from ports on VERSAFLOPPY.

2-10 DATA OUT BUFFER

The Data Out Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY from the S-100 Data Out Bus. This buffer is enabled except during input port reads from ports on VERSAFLOPPY.

2-11 BI-DIRECTIONAL DATA BUS

The Bi-Directional Data Bus is a path for all transfers to and from the I/O ports on VERSAFLOPPY.

2-12 INTERRUPT CONTROL AND VECTOR GENERATOR

At the end of each disk operation the FD1771B-1 chip asserts the INTRQ line. Interrupt Control Circuit then, priority chain permitting, asserts the PINT line back to the CPU. When the interrupt is acknowledged by the CPU (SINTA), the PINT line is released and the Interrupt Vector Generator places the Vector (or restart code) on the Data In Bus. VERSAFLOPPY operates with or without interrupts, but the standard control software does not use interrupts.

2-13 OUTPUT PORT X3 (X=6 or E)

Output Port X3 is an 8 bit control register with several functions:

1. Bits 0-3 Drive Select 1,2,3,4,
2. Bit 4 Side Select for double sided drives
3. Bit 5 Restore Drive (optional)
4. Bit 6 Wait State Circuit Enable
5. Bit 7 Interrupt Control Circuit Enable

2-14 INPUT PORT X3 (X=6 or E)

Input Port X3 is used to read the present state of several control signals:

1. Bits 0-4 State of Output Port X3, Bits 0-4
2. Bit 5 State of "double sided" jumper
3. Bit 6 State of seek complete/doubled sided signal from drive
4. Bit 7 State of INTRQ from FD1771B-1

2-15 SELECT BUFFER

The Select Buffer supplies the current sinking drive for the drive and side select lines.

2-16 CONTROL BUFFER

The Control Buffer supplies the current sinking drive for $\overline{\text{WRITE}}$ DATA, $\overline{\text{WRITE GATE}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{STEP}}$, $\overline{\text{TRK43}}$, and $\overline{\text{HLD}}$.

2-17 SENSE BUFFER

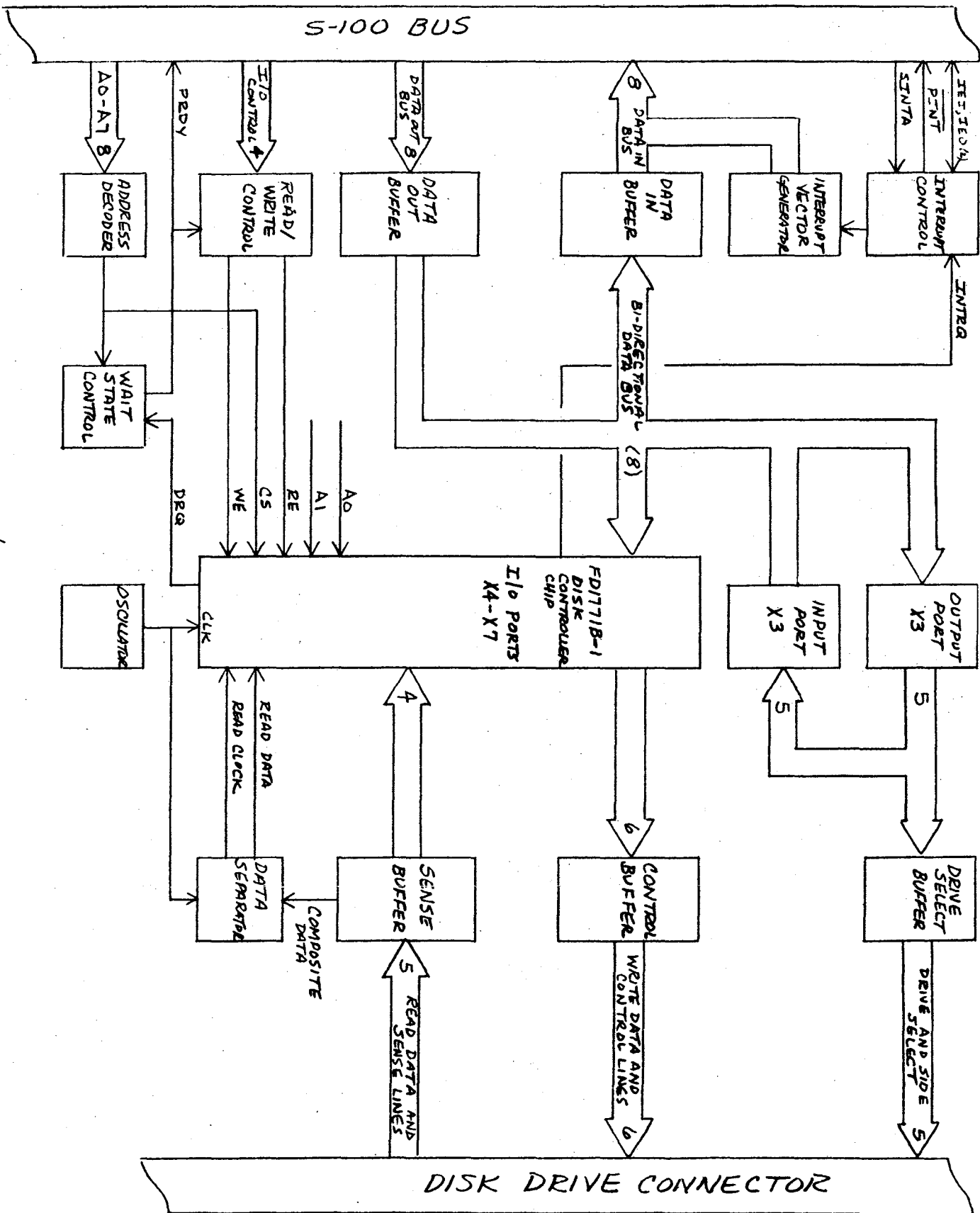
The Sense Buffer receives the $\overline{\text{READ DATA}}$, $\overline{\text{INDEX}}$, $\overline{\text{TRK00}}$, $\overline{\text{READY}}$, and $\overline{\text{WRTprt}}$ signals from the selected disk drive. Each input is a Schmitt Trigger providing hysteresis noise immunity.

2-18 DATA SEPARATOR

The Data Separator circuit divides the composite FM READ DATA into separated Data and Clock signals required by the FD1771B-1 controller chip.

2-19 OSCILLATOR

The Oscillator circuit provides a crystal controlled squarewave used by the Data Separator and FD1771B-1. This may be jumpered for mini or full size disk drive data rate.



VERSAFLOPPY BLOCK DIAGRAM
FIGURE 2-1

TABLE 2-1
S-100 BUS SIGNALS USED BY VERSAFLOPPY

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1,51	+8 Volts		
2	+16 Volts		
6	VI2	OUTPUT	OPTIONAL
14	IEI	INPUT	OPTIONAL
24	Ø2	INPUT	PHASE 2 CLOCK
29-31, 79-83	A0-A7	INPUTS	LOW ORDER ADDRESS
35,36, 38-40, 88-90	D0Ø-D07	INPUTS	DATA OUT BUS
41-43, 91-95	DIØ-DI7	OUTPUTS	DATA IN BUS
45	SOUT	INPUT	PORT OUTPUT CYCLE
46	SINP	INPUT	PORT INPUT CYCLE
64	IEO	OUTPUT	OPTIONAL
72	PRDY	OUTPUT	READY
76	PSYNC	INPUT	OPTIONAL (8085)
77	$\overline{\text{PWR}}$	INPUT	WRITE
78	PDBIN	INPUT	DATA BUS IN
96	SINTA	INPUT	INTERRUPT ACKNOWLEDG
99	$\overline{\text{POC}}$	INPUT	POWER ON CLEAR
52	-16 Volts		
100,50	GROUND		

SECTION III
CONTROL SOFTWARE

3-1 INTRODUCTION

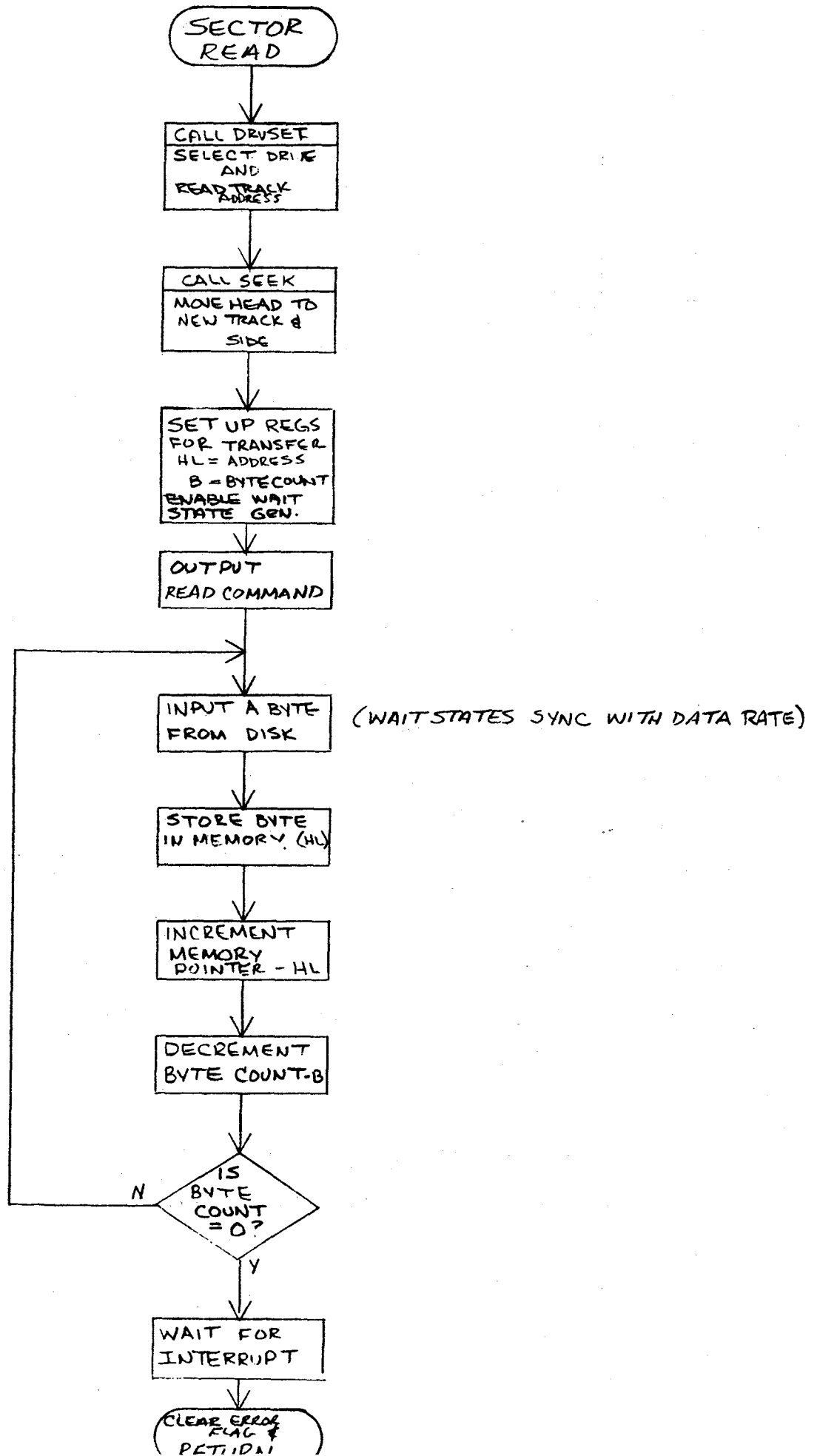
As was stated earlier, control on VERSAFLOPPY is divided evenly between hardware and the control software. Certain sequences must be executed to ensure proper operation of the disk drive. This section will cover the basic software sequences with verbal and graphic description. Program listings of the software in Z-80 source code (also runs on 8080) are included in appendix E.

The SECTOR READ and SECTOR WRITE sequences are the two main entries into the controlling software. Before these sequences may be entered, the memory transfer address, drive select, track and sector, must have been stored in memory locations. When operating with CP/M[®] Disk Operating System, these parameters are set up when the SETDMA, SELDSK, SETTRK, and SETSEC entries, respectively, are called. The READ and WRITE CP/M entries are linkages to the SECTOR READ and SECTOR WRITE sequences, respectively. (CP/M[®] is a registered trade mark of Digital Research of Pacific Grove, California.)

3-2 SECTOR READ SEQUENCE (Figure 3-1)

The function of the SECTOR READ SEQUENCE is to do everything necessary to transfer the previously specified sector (128 BYTES) to the previously specified memory buffer (anywhere in system RAM).

FIG 3-1



The DRVSET (section 3-4) and SEEK (section 3-5) subroutines are called to engage the requested drive and put the Read/Write head on the requested side and track.

The CPU registers are then set up with the memory address and byte count. Data from the disk is input a byte at a time, and stored in memory. This process is synchronized with the disk data rate by hardware inserted wait states.

When all 128 bytes of data have been read in, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occurred the program returns to the caller with the error flag cleared.

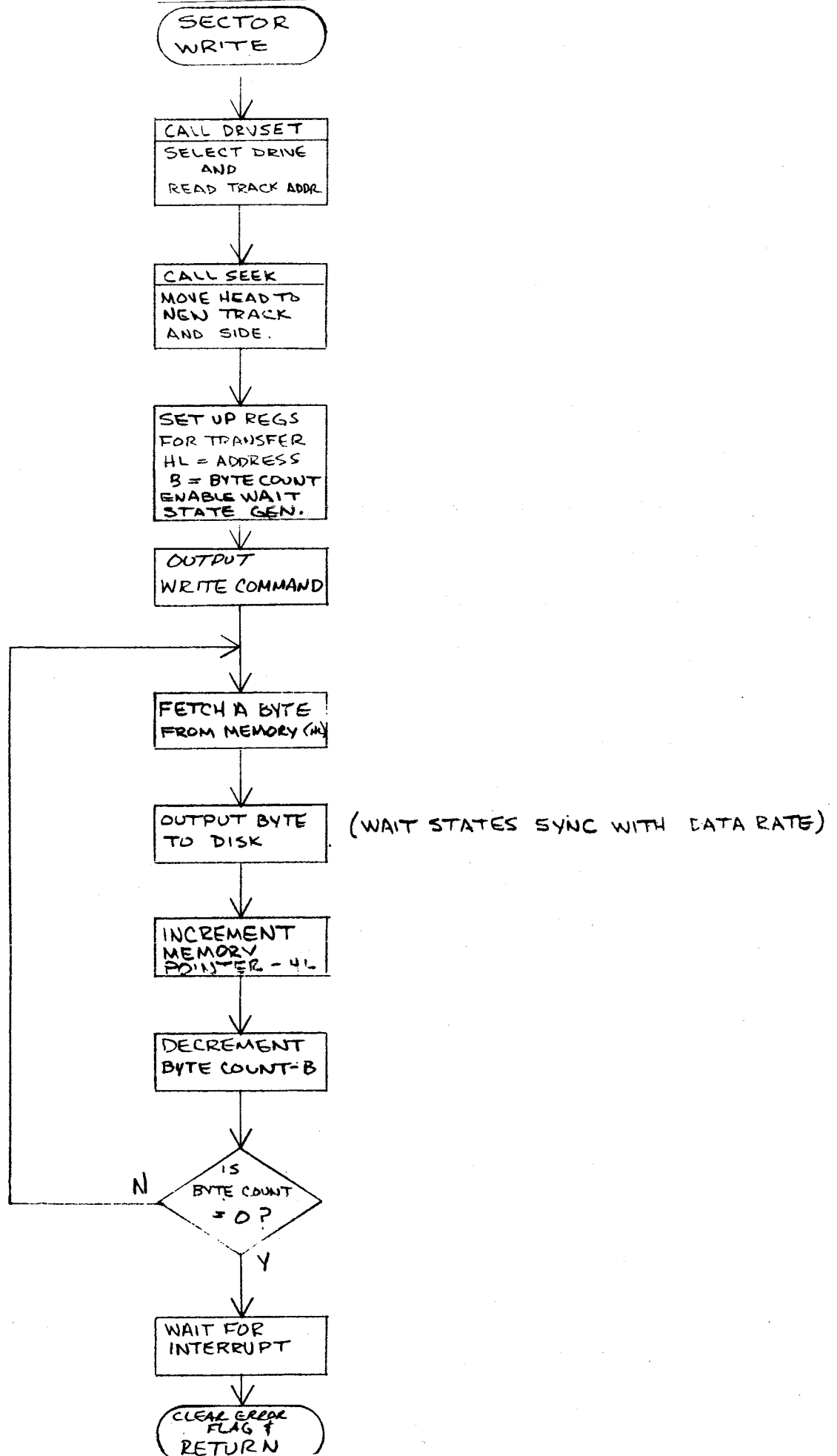
3-3 SECTOR WRITE SEQUENCE (figure 3-2)

The function of the SECTOR WRITE SEQUENCE is to do everything necessary to transfer the previously specified memory buffer (128 bytes anywhere in system) to the previously specified disk sector.

The DRVSET (section 3-4) and SEEK (section 3-5) subroutines are called to engage the requested drive and put the read/write head on the requested side and track.

The CPU registers are then set up with the memory address and byte count. The data is output a byte at a time, to the disk. This process is synchronized with the disk data rate by hardware inserted wait states.

SECTOR WRITE SEQUENCE
FIG 3-2



When all 128 bytes of data have been output, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occurred, the program returns to the caller with the error flag cleared.

3-4 DRIVE SELECTION SEQUENCE (figure 3-3)

The DRIVE SELECTION SEQUENCE checks to see if the requested drive is presently selected. If it is, the normal return is taken.

If the requested drive is not presently selected, the new selection is output followed by a 35 millisecond delay to allow for head settling.

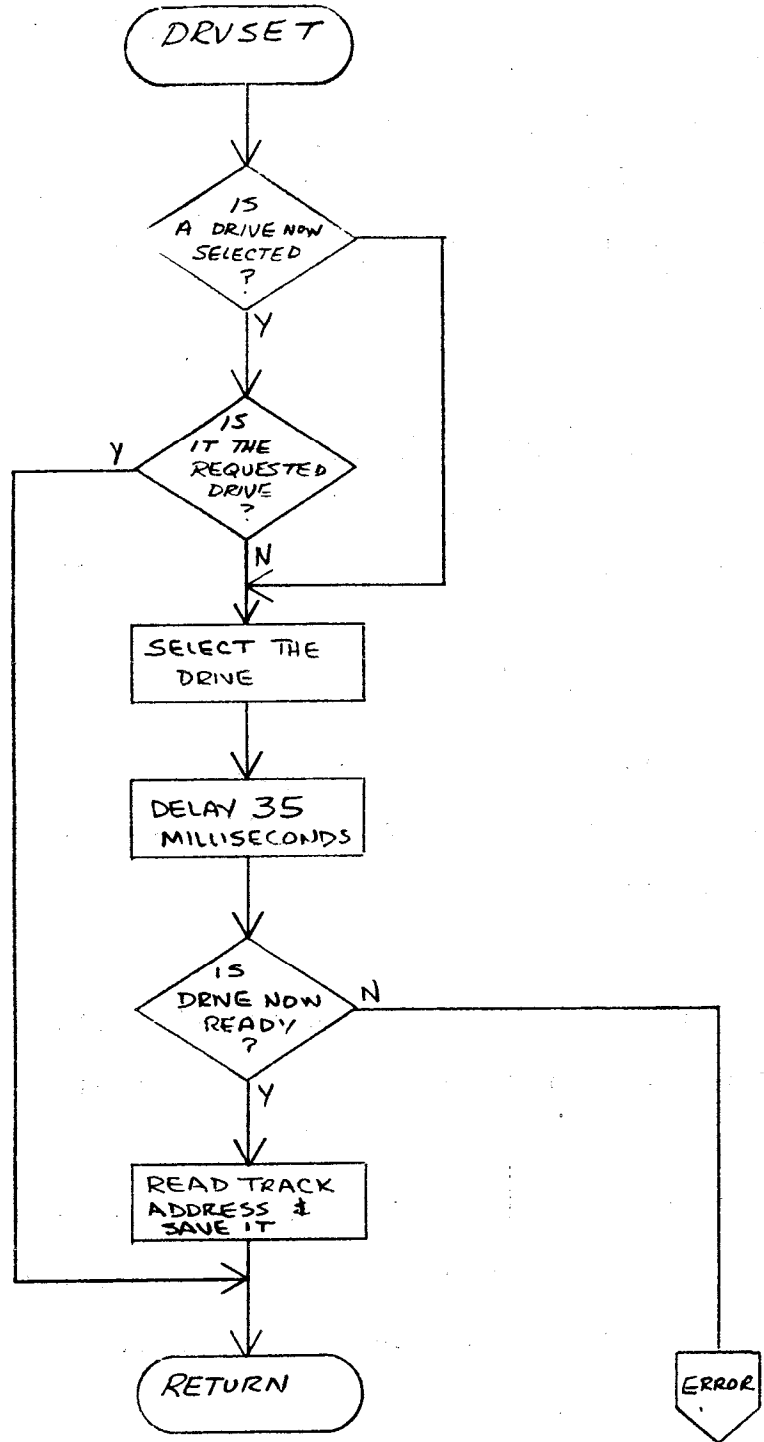
The status is then read to verify that the drive is now ready. If the drive is not ready, the error exit is taken.

If the drive is ready, the track address is read from the disk to inform the hardware of what track the new drive's read/write head is presently on. The routine normal return is then taken.

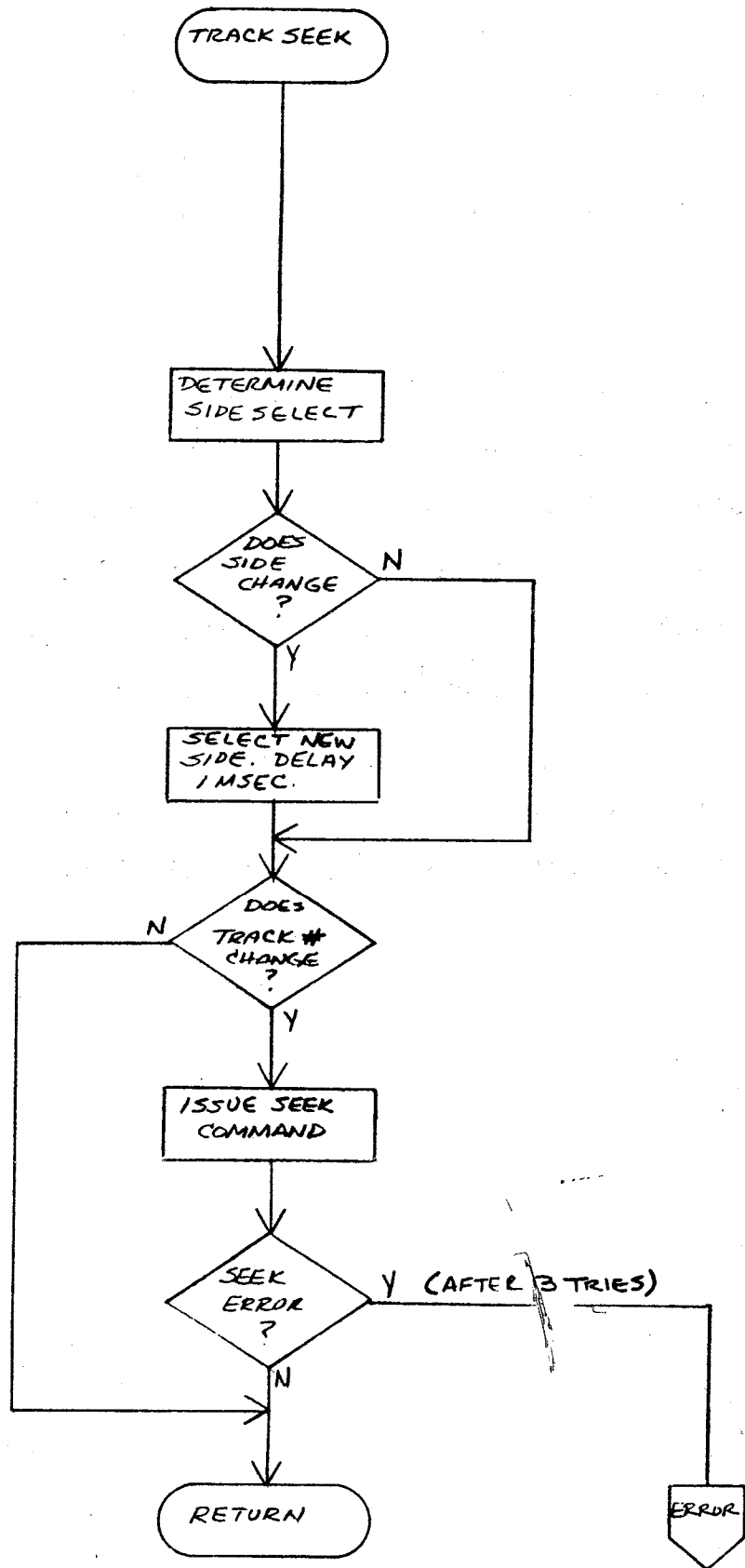
3-5 TRACK SEEK AND SIDE SELECT (figure 3-4)

The TRACK SEEK AND SIDE SELECT sequence is responsible for verifying that the requested track and sector are valid numbers, and in the case of the doublesided drives, select the proper side of the disk. Then the read/write head is moved to the requested track.

DRIVE SELECTION SEQUENCE
FIG 3-3



TRACK SEEK AND SIDE SELECT
FIG 3-4



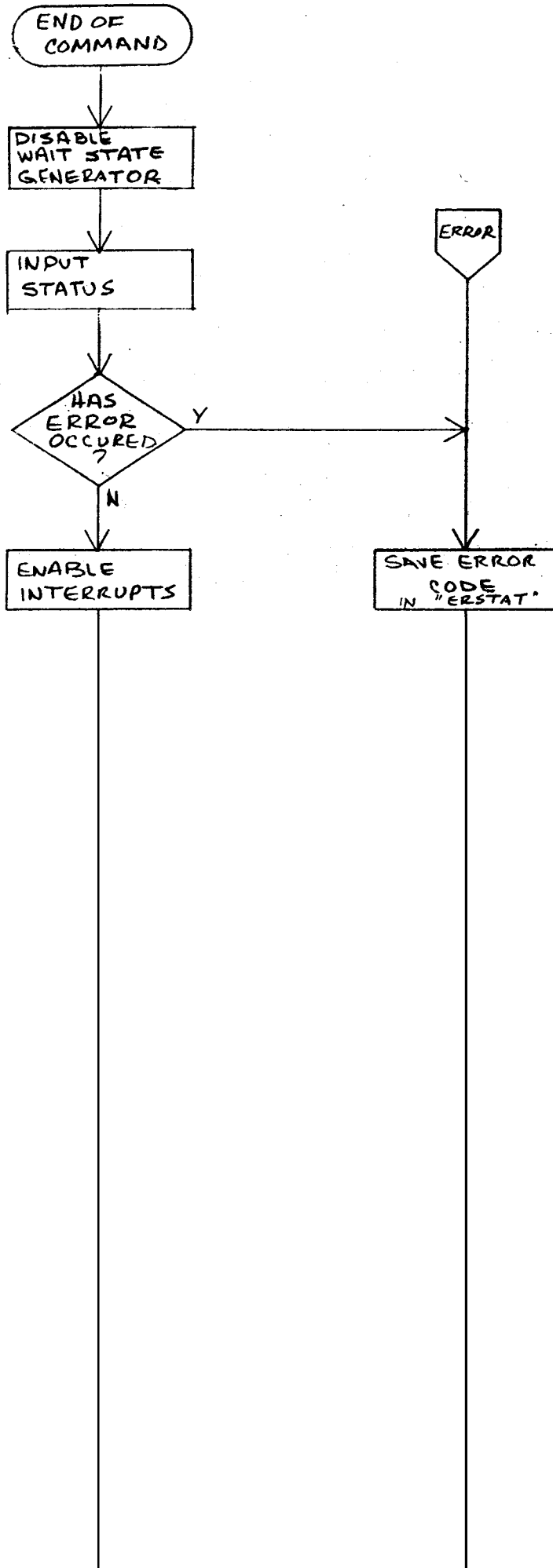
If there is a verification error after the track seek, the program moves the head to track 0 and then attempts to seek the track again. The standard control software makes two retries before taking the error exit.

3-6 END OF COMMAND ROUTINE (figure 3-5)

The END OF COMMAND ROUTINE is entered after both normal and error terminations of hardware executed commands. The routine waits for the FD 1771B-1 to become "not busy". The wait state generator is then disabled, and the status is input to check for errors. If no error occurred, then a normal return is taken.

If an error condition is detected, the error type is saved, error flag set and a return is taken directly back to the caller.

END OF COMMAND ROUTINE
FIG 3-5



SECTION IV
CONSTRUCTION

4-1 INTRODUCTION

The SD SALES Floppy Disk Controller Board Kit is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category it is highly recommended that you either:

1. Find an experienced person to help you in assembly and check out the board or
2. Return the board to SD SALES and have the board assembled and tested.

Appendix B shows the parts list for the SD SALES Floppy Disk Controller board. Double check all parts against this parts list. If any differences are noted, please call SD SALES at 1-800-527-3460. (Toll free). NOTE: General construction information, assembly diagram and schematic diagram can be found in the Appendices.

4-2 ASSEMBLY PROCEDURE

1. Install the IC sockets in their proper locations.

NOTE: No socket for DIP switch U29.

2. Install the resistors as follows:

- A. R1,R12,R14, 10K Ohm $\frac{1}{4}$ W 10% (Brown,Black,Orange)
- B. R2,R5,R6,R7,R8,R11 3.3K Ohm $\frac{1}{4}$ W 10% (Orange,Orange,Red)
- C. R3,R4, 820 Ohm $\frac{1}{4}$ W 10% (Gray,Red,Brown)
- D. R9 390 Ohm $\frac{1}{2}$ W 10% (Orange,White,Brown)
- E. R10 120 Ohm $\frac{1}{2}$ W 10% (Brown,Red,Brown)
- F. R13 150 Ohm $\frac{1}{4}$ W 10% (Brown,Green,Brown)
- H. RP 1 Resistor pack 3.3K Ohm 10 pin SIP

NOTE: Pin 1 of this SIP is designated by a notch or a dot on the end of this package.

3. Install diodes CR1 and CR2 with the banded end as shown on the PC board.
 - A. CR1 Zener diode 1N751-5V
 - B. CR2 Zener Diode 1N472A-12V

4. Install the capacitors as follows:
 - A. C1,C16,C17,C22,C23 10MF TANTALUM (note proper polarity)
 - B. C2-C5,C8-C15 0.1 MF CERAMIC
C18-C21
 - C. C6 10PF MICA
 - D. C7 .01 MF CERAMIC

5. Install the voltage regulator with this heat sink, using the 6-32 hardware supplies.

VR1 +5V 7805/LM340T-5

6. Install the BERG HEADERS (On top side of board with long portion of Pin Up.)
 - A. Install BERG 2 Pin Headers in the following locations:

E13-E14
E19-E20
E24-E25
E30-E31
E35-E36
E37-E38
E39-E40
E41-E42
E43-E44

 - B. Install BERG 3 Pin Headers in the following locations:
 - a. E1,E2,E3
 - b. E4,E5,E6
 - c. E10,E11,E12
 - d. E16,E17,E18
 - e. E21,E22,E23
 - f. E26,E27,E28
 - g. E32,E33,E34

 - C. Install BERG 4 Pin Header in E7,E8,E9,E29

 - D. Install BERG 1 Pin Header in E15

7. Double check all solder connections for cold solder joints, unsoldered connections or shorted connections.

4-3 VOLTAGE CHECK

1. Install the board in the computer and measure the output of +5V regulator VR1, -5V and +12V of CR1 and CR2 respectively.
 - A. VR1 = +5V (Bottom Pin)
 - B. CR1 = -5V (Anode)
 - C. CR2 = +12V (Cathode)
2. Measure the power supply voltages in the Floppy Disk Controller chip (any of the IC socket can be used.)
 - A. Pin 1 U16 = -5V
 - B. Pin 21 U16 = +5V
 - C. Pin 40 U16 = +12V

NOTE: Do not proceed with board check out until all power supply voltages are correct. The TTL and MOS Logic can be permanently damaged if improper voltages are applied.

3. Install the IC's in their sockets observing the Pin 1. designation on each socket marked on the PC board.

A. U2,U20	74LS10
B. U3,U8	74LS08
C. U4	74LS38
D. U5	Resistor 14 Pin MDL DIP 150 Ohm
E. U6,U18,U24	74LS244
F. U7,U9	7406
G. U14,U25	74LS14
H. U11	74LS193
I. U12,U13,U19,U1	74LS74
J. U15	74LS122
K. U16	FD1771B-1
L. U17	74LS273
M. U21	74LS02
N. U22,U23	74LS21
O. U26,U27,U28	74LS40
P. U29	Dip Switch 8 Position
Q. U10	74LS04
4. Double check all IC's for proper orientation and location.
5. Refer to JUMPER OPTION SECTION V for proper configuration of jumper options and connect jumpers as required.

SECTION V

JUMPER OPTION SELECTION/INSTALLATION

5-1 INTRODUCTION

VERSAFLOPPY has been designed to accomodate a variety of disk drives and S-100 Z-80 and 8080 CPU boards. Care should be taken to install the correct jumpers for the user's specific computer system configuration. BERG PV Jumpers have been included for quick jumper installation and changes.

5-2 I/O PORT ADDRESS SELECTION

VERSAFLOPPY uses five I/O port address and these may reside at one of two possible places: 63H-67H (X=6) or E3_H - E7_H (X=E). Install the jumper for X=6 when using VERSAFLOPPY with the standard control software.

X	PORT ADDRESS	JUMPER
X=6	63H - 67H	E33-E34
X=E	E3H - E7H	E32-E33

5-3 CPU SELECTION

VERSAFLOPPY operates with Z-80, 8080 and 8085 CPU boards. Install all of the jumpers for the CPU to be used as follows:

CPU	JUMPERS
IMSAI/ALTAIR 8080	E24-E25, E27-E28
SDS Z-80	E27-E28
SBC-100	E27-E28
IMSAI 8085	E24-E25, E26-E27, E43-E44

5-4 INTERRUPT OPTIONS

There are several possible methods of handling interrupts with VERSAFLOPPY:

1. Interrupts not used. (Standard Software)
2. 8080 Mode using on board restart code.
3. 8080 Mode using a priority interrupt controller board.
4. Z-80 Mode 2 using on board vector code.
5. Z-80 Mode 2 using CTC interrupt circuit on SBC-100.

The Standard Control Software does not use interrupts. However in some cases it may be beneficial to inssue a command (such as seek track) and be interrupted when it is complete. When interrupts are used , VERSAFLOPPY must be given HIGHEST PRIORITY during SECTOR READS and SECTOR WRITES. An interrupt priority chain has been implemented for systems containing multiple sources of in-terrupts. This chain uses pin 14 for IEI (Interrupt Enable In) and pin 64 for IEO (Interrupt Enable Out). These will have to be used in conjunction with an S.D.S. motherboard which supports this chain.

The following table lists the jumpers for interrupt options:

INTERRUPT MODE	JUMPERS
INTERRUPTS NOT USED	NONE
8080 Mode Restart on board	E37-E38
8080 Mode using external controller	E13-E14 (uses VI2)
Z80 Mode 2 Using on board Vector	E37-E38
Z80 Mode 2 Using Off board CTC	E13-E14 (uses VI2)
If Priority Chain is used add	E30-E31 & E35-E36

5- 5 DRIVE SELECTION

VERSAFLOPPY operates with several of the available floppy disk drives. Install the jumpers for the type of drive which is to be used.

DRIVE TYPE	JUMPERS
1 Shugart SA400	E22-E23, E1-E2, E41-E42, E16-E17
2 Shugart SA450	E22-E23, E1-E2, E19-E20, E41-E42, E16-E17
3 Shugart SA800 MFE 700, CDC9404*	E21-E22, E7-E8, E4-E5, E10-E11, E15-E17
4 Shugart SA850 MF 750, CDC9406*	E21-E22, E19-E20, E7-E8, E4-E5, E10-E11, E15-E17
5 Persci 70	E21-E22, E17-E18, E39-E40, E4-E5, E10-E11
6 Persci 277	E21-E22, E17-E18, E5-E6, E11-E12, E39-E40
7 GSI GS-105	Same as SA800 Plus E9-E29

* CDC Drives are not Pin for Pin compatible and require a Non Standard Cable.

SECTION VI
SOFTWARE OPTIONS

6-1 INTRODUCTION

The standard control software for VERSAFLOPPY is supplied in listing form (Appendix D) and also available in 2708 or 2758 PROM for an additional charge. This software is called BIOS (Basic I/O System) and is linked to the S.D. Modified CP/M disk operating system (Section 6-4) to reside at F000H. There are several parameters within BIOS that must be set up for the particular computer environment in which the VERSAFLOPPY is to operate.

6-2 CONSOLE PORT ADDRESS AND BIT MASKS

The minimum I/O configuration for CP/M to operate is a disk drive and a console or terminal. BIOS is set up to talk to the console via a UART type of interface. The port address of the UART (Data and STATUS) must be set up to match that of the console in the system. The following bytes within BIOS (version 1.0) must be set up:

<u>ADDRESS</u>	<u>DESCRIPTION</u>
F06B	Console Input Status Port Address
F06D	Console Input Data Ready Mask (RDA)
F079	Console Input Data Port Address
F07E	Console Output Status Port Address
F080	Console Output Ready Mask (TBE)
F086	Console Output Data Port Address

If a special type of console device, such as a VDM, is to be used, the following mods will allow jumping to the users software driver:

ADDRESS	DATA	DESCRIPTION
F006	.C3	Console Input Status Linkage-
F007	Low Order Address	This routine checks the console
F008	High Order Address	input to see if a character is ready to be read in. If a character is ready, return with ACC=FF. If not, ACC=0.
F009	C3	Console Input Linkage- This routine
F00A	Low Order Address	must input character from console
F00B	High Order Address	keyboard and return it in ACC.
F00C	C3	Console Output Linkage -
F00D	Low Order Address	This routine must output the
F00E	High Order Address	charater in C-reg to console.

6-3 DRIVE PARAMETER OPTIONS

Several software parameters must be set up for the type of drive (mini or full size) to be used:

<u>ADDRESS</u>	<u>DATE (HEX)</u>		<u>DESCRIPTION</u>
	<u>MINI</u>	<u>FULL SIZE</u>	
F03F	12	1A	Sectors per track
F040	23	4D	Tracks per side
F041	14	4C	Format Gap 1
F042	11	11	Format Gap 2
F043	0E	21	Format Gap 3
F044	03	0A	Restore Command
F045	17	1E	Seek Command
F046	13	1A	Seek with no verify
F047	4B	23	Head Load Delay

6-4 CLOCK RATE PARAMETER

The following byte must be set up for the system clock rate.

<u>ADDRESS</u>	<u>2MHZ</u>	<u>2.5MHZ</u>	<u>3MHZ</u>	<u>4MHZ</u>
F048	8E	B2	D8	00

6-5 BOOTING UP CP/M

In order to run CP/M disk operating system, a minimum of 16K of RAM must be in the system starting at address 0000 and the BIOS PROM must be at F000_H. Execute BIOS at F000 and CP/M will be booted and prompt with "A>". Refer to the "AN INTRODUCTION TO CP/M FEATURES AND FACILITIES" manual for details of the CP/M commands.

SECTION VII

CHECK - OUT

7-1 INTRODUCTION

This section will describe some basic checks that should be made on the VERSAFLOPPY. NOTE: It is assumed at this point that the voltage checks described in Section 4 have been previously made. The following checks require that the CPU board also be plugged in to the Bus. Be sure to check all jumper options.

7-2 OSCILLATOR

Apply power to board and verify that there is a 4MHZ clock on E21.

7-3 \overline{RE} AND \overline{WE} PULSES

Verify that U16 Pin 4 pulses low during any Input instruction, and U16 Pin 2 pulses low during any output instruction.

7-4 I/O PORT WRITE/READ VERIFICATION

Using the monitor in the system or a short program, write data to port X5 (x=6 or E) and read it back. Verify that the data read back is the same as that written. This is done to test the

data path to and from the FD1771B-1 as well as the internal register. REPEAT this procedure for ports X6 and X7. Bits 0-4 of port X3 should also read back data that is written to them.

7-5 HEAD LOAD MONOSTABLE

After the diagnostic software is operating, check E15 for a 35 millisecond pulse (low) each time the head loads. This need not be tested when using mini drives.

SECTION VIII
DIAGNOSTIC SOFTWARE

8-1 INTRODUCTION

A diagnostic program for VERSAFLOPPY is supplied in listing form (APPENDIX E) and also available in 2708 or 2758 PROM for an additional charge. The diagnostic program is also on the diskette, when CP/M is purchased, under the file name of "VDIAG.COM". Once CP/M is operating, the diagnostic may be run by typing VDIAG (CR). The CP/M diskette should not be placed in the drive until the VERSAFLOPPY and disk drive(s) have been thoroughly checked out.

When running the diagnostic to check-out the VERSAFLOPPY, insert the PROM containing the diagnostic program in a PROM board which is addressed above the RAM. (16K minimum starting at 0000). Copy the contents (1K) of the PROM to the 1K block of memory starting at 100H. The diagnostic uses the BIOS PROM for disk and console I/O, which must have been set up as described in Section VI.

8-2 DIAGNOSTIC TEST START-UP

Execute the diagnostic program at 100H and the following message will print on the console:

TEST # DRV # (TTDD)

The program then waits for the test number and drive number to be entered from the console followed by a carriage return. NOTE: The test number and drive number are each two digits and MUST NOT be separated by a comma or space.

The test routines may be terminated at any time by entering a period (.) on the console keyboard. The diagnostic will then print the above prompting message and wait for further keyboard entries.

8-3 DIAGNOSTIC TEST 00 (SEEK TEST)

Test 00 is a simple routine to verify that the VERSAFLOPPY is receiving commands properly and that the track seek circuitry is functional. The selected drive should begin moving the head from track 00 to the inside track (76 for full size, 34 for mini) and back again. Enter a period on the keyboard to cause the test to cease.

8-4 DIAGNOSTIC TEST 01 (WRITE/READ)

Diagnostic test 01 writes random data on each sector, reads the sector back and compares the data to verify that it is identical. Any errors which occur will be printed on the console. (see section 8) This is done to each sector sequentially, starting at track 00, sector 1, until reaching the innermost track. At that point it prints a "P" on the console, returns to track 00, and continues. Enter a period (.) to terminate this test.

NOTE: Diagnostic tests which read and write to disk may only be run after the diskette has been formatted using diagnostic 05. (See 8-8)

8-5 DIAGNOSTIC TEST 02 (READ TEST)

Test 02 reads every sector on the disk sequentially and checks for CRC errors, and seek errors. Errors will be reported on the console. This test should step from track to track at the same rate as when formatting a diskette.

8-6 DIAGNOSTIC TEST 03 (RANDOM WRITE/READ)

This test is similar to test 01 in that it writes, reads and compares data byte by byte. However, test 03 chooses the sectors on a random basis in an attempt to simulate actual use. This test exercises only the specified drive.

8-7 DIAGNOSTIC TEST 04 (MULTI-DRIVE RANDOM WRITE/READ)

This test is identical to Test 03 except that it also selects a random drive (0 or 1)

8-8 DIAGNOSTIC TEST 05 (FORMATTING)

Test code 05 is actually not a diagnostic, but a program which formats a diskette with the IBM 3740 soft sectored data. This

must be done to all diskettes before further use. Note that on the distributed CP/M diskette there is a program which formats a diskette in drive B. This program has the filename "FORMAT.COM" and may be run by entering "FORMAT (CR)". Be sure to have a scratch or unformatted diskette in drive B when "FORMAT" is run because any previously written data will be lost.

8-9 DIAGNOSTIC TEST 10 (LOAD FROM DISK)

Test code 10 is not a diagnostic, but provides a means of loading absolute sectors into memory. Note the following interactive sequence: (all user entries are underlined)

<u>CONSOLE INTERACTION</u>	<u>COMMENTS</u>
TEST # DRV # (TTDD) : <u>1000</u> (CR)	Test code 10, Drive 00
ENTER LOAD ADDR: <u>2000</u> (CR)	Memory address for load=2000 _H
ENTER TRACK/SECTOR (TTSS): <u>1205</u> (CR)	Start at TRK12, Sector 05
ENTER NUMBER OF SECTORS (NN): <u>20</u> (CR)	Load 20 _H sectors

At this point, 20_H Sectors (32 x 128 bytes) starting at track 12_H sector 5 would load into memory starting at address 2000_H.

8-10 DIAGNOSTIC TEST 11 (SAVE ON DISK)

Test code 11 provides a means of saving the contents of memory on disk. The following sequence describes this:

<u>CONSOLDE INTERACTION</u>	<u>COMMENTS</u>
TEST # DRV # (TTDD) : <u>1100</u> (CR)	Test code 11, drive 00
ENTER SAVE ADDR: <u>2000</u> (CR)	Memory address for save=2000 _H
ENTER TRACK/SECTOR (TTSS): <u>1205</u> (CR)	Start at Track 12 _H Sector 05
ENTER NUMBER OF SECTORS (NN): <u>20</u> (CR)	Save 20 _H sectors

At this point, 20_H sectors (32 x 128 bytes) would be written to disk from memory starting at address 2000_H.

8-11 DIAGNOSTIC TEST FF (JUMP)

Test code FF allows executing the diagnostic to anywhere in memory. The following sequence describes this:

<u>CONSOLE INTERACTION</u>	<u>COMMENTS</u>
TEST #, DRV # (TTDD): <u>F000</u> (CR)	
ADDRESS: <u>3000</u> (CR)	Jump to address 3000 _H

8-12 DIAGNOSTIC ERROR REPORTING

If any errors occur during diagnostics 1,2,3, or 4, the errors will be reported on the console as follows:

CMD STAT DRV TRK SCTR> CC SS DD TT SS

where CC = The controller command being executed
SS = The error status (type of error)
DD = The drive being tested
TT = The track being tested
SS = The sector being tested

Table 8-1 lists the various controller commands and table 8-2 contains the definition of each bit in the error status byte.

TABLE 8-1
DISK CONTROLLER COMMAND CODES

MINI DISK CMD CODE	FULL SIZE CMD CODE	DESCRIPTION
03	0A	Restore Drive to TRK 00
17	1E	Track Seek
13	1A	Track Seek with No Verify
F4	F4	Format Track
88	88	Read Sector
8C	8C	Load Head, Then Read Sector
A8	A8	Write Sector
AC	AC	Load Head, Then Write Sector
C4	C4	Read Track Address

TABLE 8-2
ERROR STATUS DEFINITION

BIT #	DEFINITION
BIT 0	Write Deleted Sector has been read
BIT 1	DRQ Bit (Indicates Excessive noise on S100 Bus)
BIT 2	Data Lost
BIT 3	CRC Error
BIT 4	Sector Not Found
BIT 5	Track Seek Error
BIT 6	Write Protected Diskette
BIT 7	Drive Not Ready

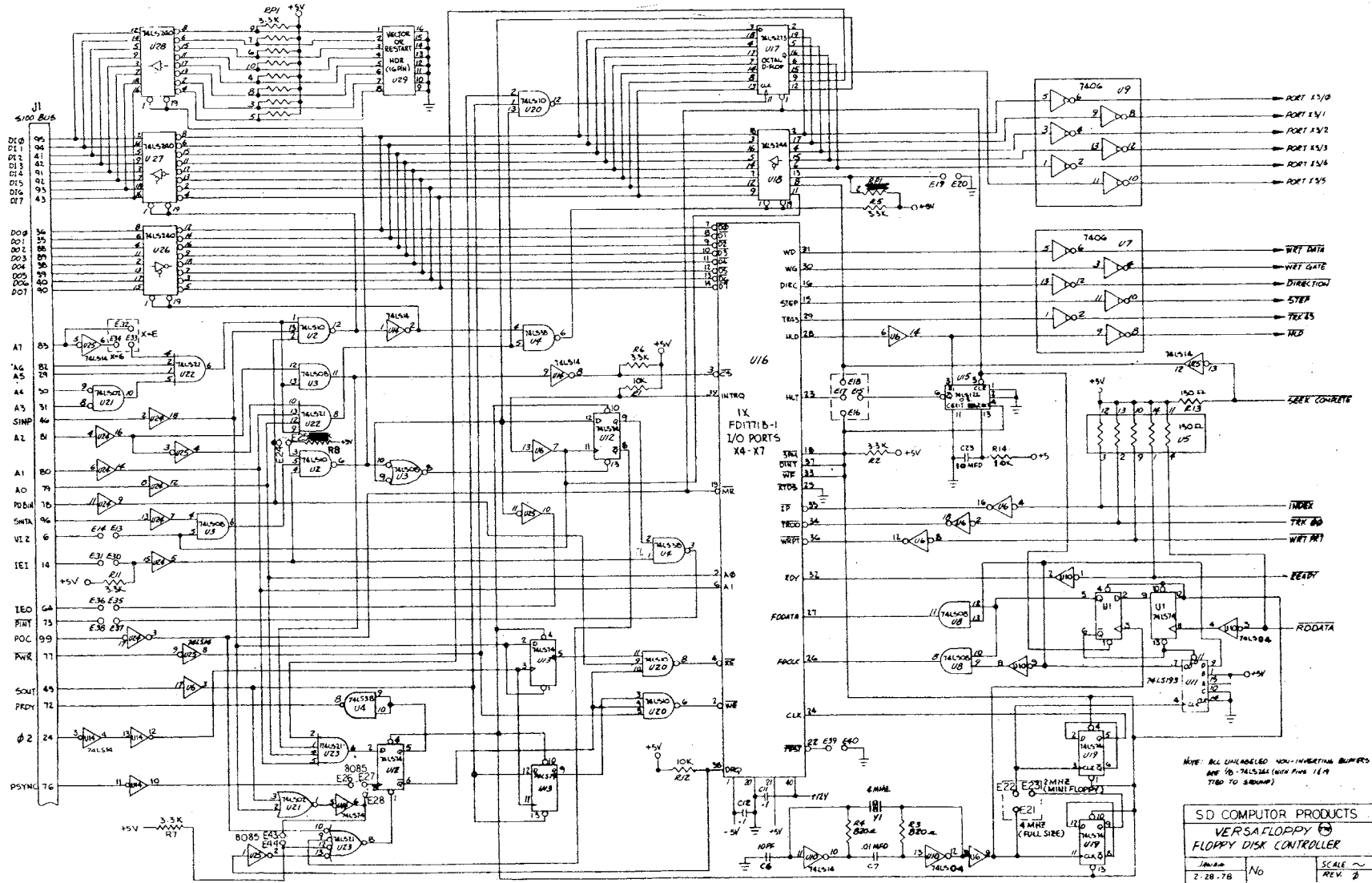
APPENDIX A

FLOPPY DISK CONTROLLER PARTS LIST

<u>ITEM #</u>	<u>QUANTITY</u>	<u>DESCRIPTION</u>	<u>LOCATION</u>
1	1	P.C. BOARD	
2	1	74LS02	U21
3	1	74LS04	U10
4	2	74LS08	U3,U8
5	2	74LS10	U2,U20
6	2	74LS14	U14,U25
7	2	74LS21	U22,U23
8	1	74LS38	U4
9	4	74LS74	U1,U12,U13,U19
10	1	74LS122	U15
11	1	74LS193	U11
12	3	74LS240	U26,U27,U28
13	3	74LS244	U6,U18,U24
14	1	74LS273	U17
15	2	7406	U7,U9
16	1	FD 1771B-1	U16
17	1	DIP SWITCH, 8 POSITION	U29
18	18	SOCKET, 14 PIN	
19	1	SOCKET, 16 PIN	
20	7	SOCKET, 20 PIN	
21	1	SOCKET, 40 PIN	
22	1	RESISTOR MDL, 14 PIN DIP 150 Ohm	U5
23	1	RESISTOR MDL, 10 PIN SIP 3.3K	RP1
24	3	RESISTOR, 10K, 1/4W, 10%	R1,R12,R14
25	6	RESISTOR, 3.3K, 1/4W, 10%	R2,R5-R8,R11
26	2	RESISTOR, 820 Ohm, 1/4W 10%	R3,R4
27	1	RESISTOR, 150 Ohm, 1/4W, 10%	R13
28	1	RESISTOR, 120 Ohm, 1/4W, 10%	R10
29	1	RESISTOR, 390 Ohm, 1/4W, 10%	R9
30	5	CAPACITOR, 10 MFD, 20V TANT.	C1,C16,C17,C22,C23
31	16	CAPACITOR, .1 MFD, 16V MONOCERAMIC	C2-C5,C8-C15, C18-C21
32	1	CAPACITOR, .01 MFD, 16V CERAMIC	C7
33	1	CAPACITOR, 10 PFD, 16V MICA DIP	C6
34	1	ZENER DIODE, 1N751 5V	CR1
35	1	ZENER DIODE, 1N4742A, 12V	CR2
36	1	LM340T-5 VOLTAGE REGULATOR, 5V	VR1
37	12	BERG 65474 PV JUMPERS	
38	1	HEAT SINK, 6106-14	
39	1	4 MHz CRYSTAL	Y1
40	1	BERG 65500-401 STRAIGHT HEADER (1PIN)	E15
41	9	BERG 65500-402 STRAIGHT HEADER (2PIN)	E13,E19,E24,E30 E55,E37,E39,E41 E43
42	7	BERG 65500-403 STRAIGHT HEADER (3PIN)	E1,E4,E10,E16 E21,E26,E32
43	1	BERG 65500-404 STRAIGHT HEADER (4PIN)	E7

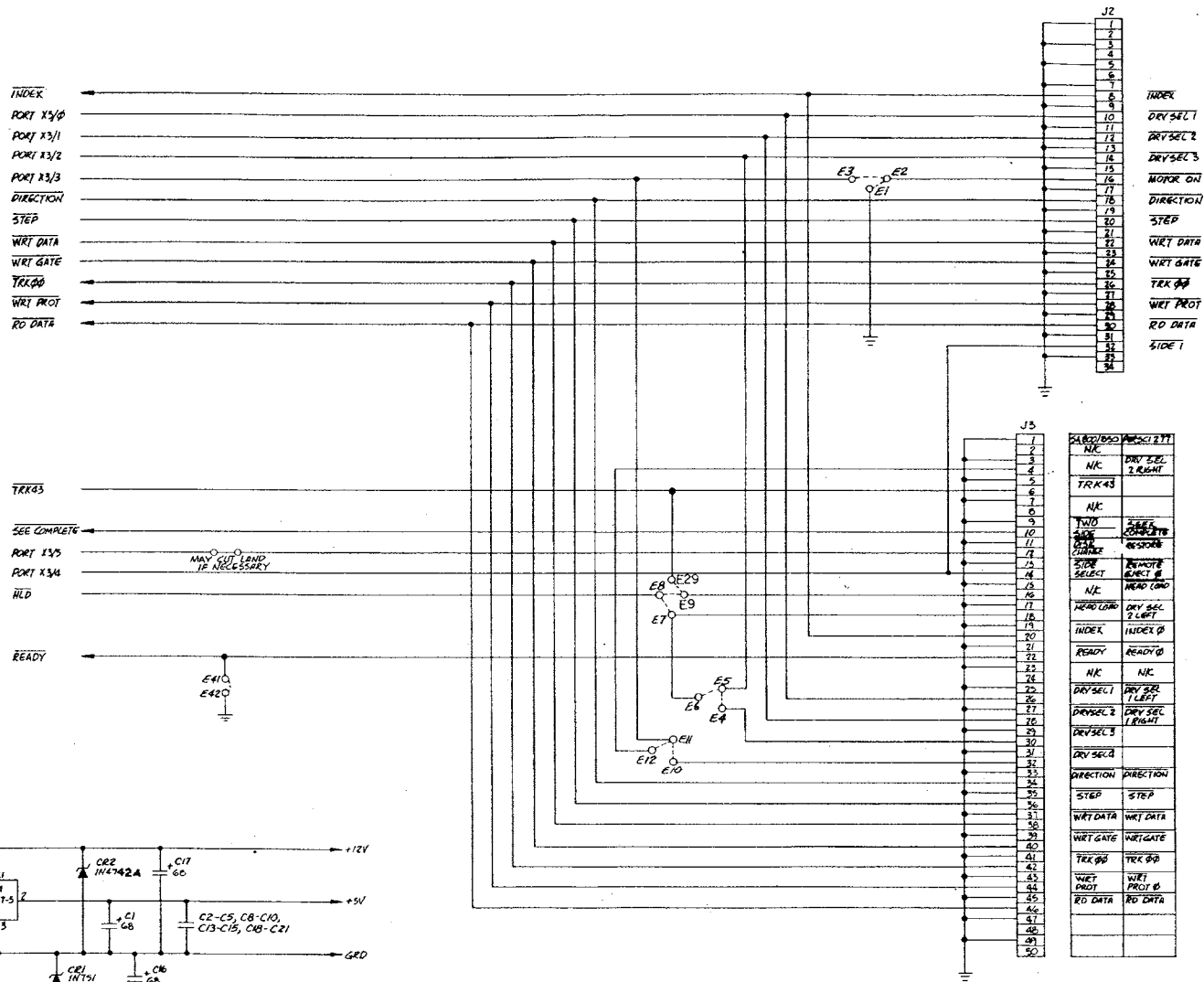
APPENDIX B

VERSAFLOPPY SCHEMATIC
DIAGRAM



NOTE: ALL UNLABELED NON-INVERTING BUFFERS ARE 74LS244 (WITH PINS 1 & 4 TIED TO GROUND)

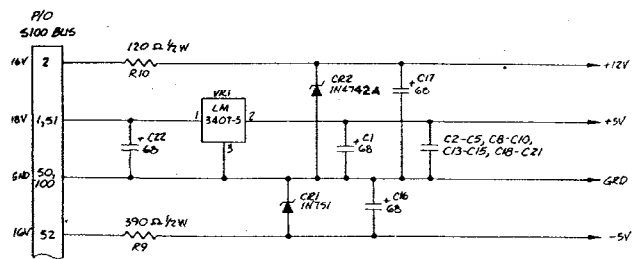
S.D. COMPUTER PRODUCTS
 VERSAFLOPPY
 FLOPPY DISK CONTROLLER
 2-28-78 No SCALE ~
 REV. 2



TO 5A400/450

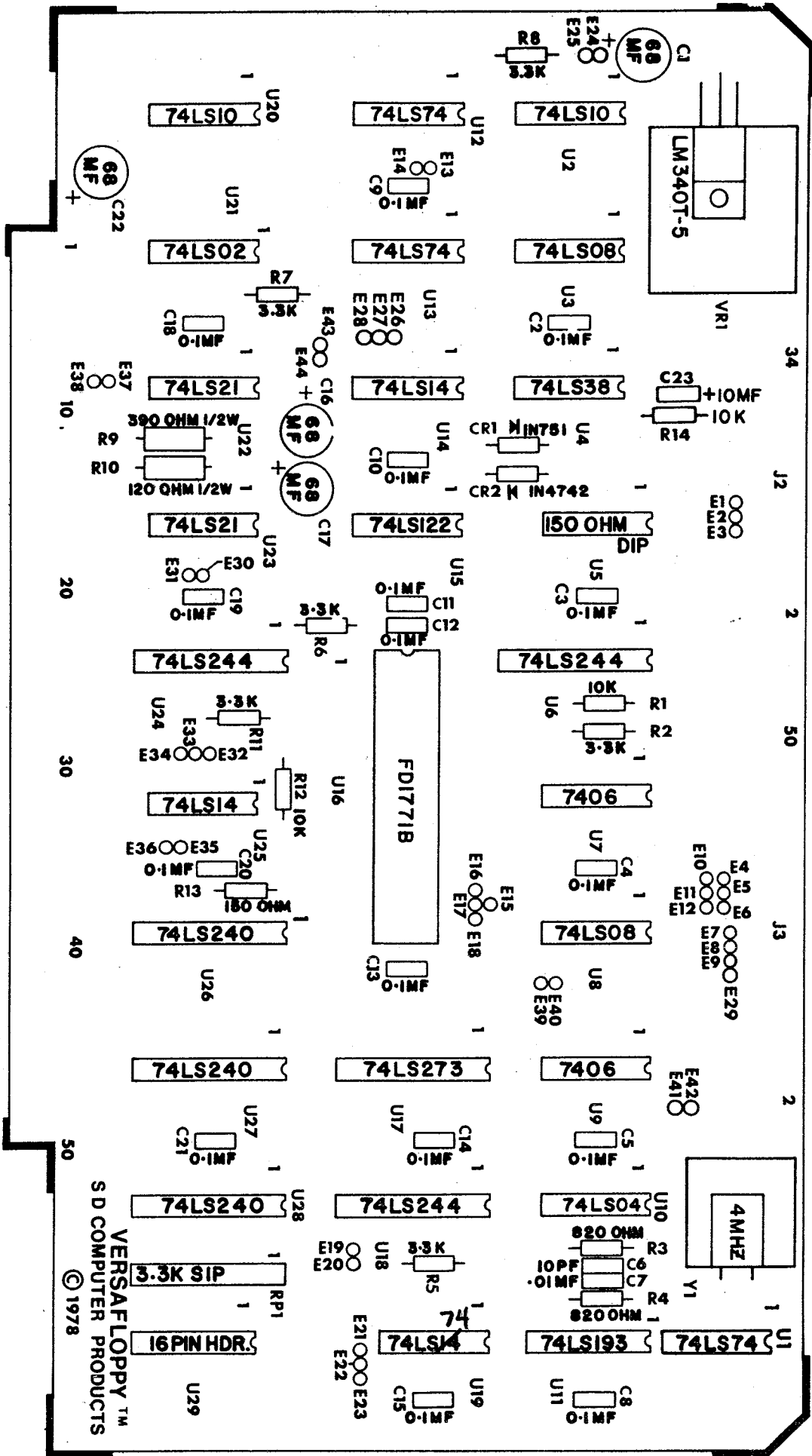
TO 5A800/050
MFE
PERSCI 277
CPC 9404/6 *

* REQUIRES CABLE ADAPTER



J2	J3	PERSCI 277
1	1	NK
2	2	NK
3	3	DRY SEL 2 RIGHT
4	4	TRK 03
5	5	NK
6	6	NK
7	7	TWO
8	8	DRY SEL 1 LEFT
9	9	DRY SEL 2 LEFT
10	10	DRY SEL 3
11	11	DRY SEL 4
12	12	DRY SEL 5
13	13	DRY SEL 6
14	14	DRY SEL 7
15	15	DRY SEL 8
16	16	DRY SEL 9
17	17	DRY SEL 10
18	18	DRY SEL 11
19	19	DRY SEL 12
20	20	DRY SEL 13
21	21	DRY SEL 14
22	22	DRY SEL 15
23	23	DRY SEL 16
24	24	DRY SEL 17
25	25	DRY SEL 18
26	26	DRY SEL 19
27	27	DRY SEL 20
28	28	DRY SEL 21
29	29	DRY SEL 22
30	30	DRY SEL 23
31	31	DRY SEL 24
32	32	DRY SEL 25
33	33	DRY SEL 26
34	34	DRY SEL 27
35	35	DRY SEL 28
36	36	DRY SEL 29
37	37	DRY SEL 30
38	38	DRY SEL 31
39	39	DRY SEL 32
40	40	DRY SEL 33
41	41	DRY SEL 34
42	42	DRY SEL 35
43	43	DRY SEL 36
44	44	DRY SEL 37
45	45	DRY SEL 38
46	46	DRY SEL 39
47	47	DRY SEL 40
48	48	DRY SEL 41
49	49	DRY SEL 42
50	50	DRY SEL 43

VERSAFLOPPY PARTS PLACEMENT DRAWING



VERSAFLOPPY™
 SD COMPUTER PRODUCTS
 © 1978

APPENDIX D
VERSAFLOPPY CONTROL
SOFTWARE
"BIOS"

```

0002          NAME      BIOS
0003 ;
0004 ;          I/O DRIVERS FOR CP/M
0005 ;
0006 ;          VERSION 1.0      03/17/78
0007 ;          RUNS ON Z80, 8080, OR 8085
0008 ;
0009          PSECT     ABS
>F000        0010          ORG      0F000H
0011 ;
0012 ;
>0080        0013 NBYTES  EQU      128      ; BYTES PER SECTOR
0014 ;
0015 ;
>0000        0016 RBASE   EQU      0000H      ; START OF RAM
>0040        0017 TADDR   EQU      RBASE+40H   ; TRANSFER ADDRESS
>0042        0018 UNIT    EQU      RBASE+42H   ; DRIVE #
>0043        0019 SCTR    EQU      RBASE+43H   ; SECTOR
>0044        0020 TRK     EQU      RBASE+44H   ; TRACK
>0045        0021 NREC    EQU      RBASE+45H   ; # OF SECTORS
>0046        0022 ERMASK  EQU      RBASE+46H   ; ERROR MASK
>0047        0023 ERSTAT  EQU      RBASE+47H   ; ERROR STATUS
>0048        0024 IDSV    EQU      RBASE+48H   ; 4 BYTES
>004C        0025 CMDSV   EQU      RBASE+4CH   ; COMMAND SAVE
>004D        0026 SPSV    EQU      RBASE+4DH   ; SP SAVE (2 BYTES)
>0080        0027 SSTACK  EQU      RBASE+80H   ; SYSTEM STACK
>0080        0028 COLD    EQU      RBASE+80H   ; COLD START ADDRESS
0029 ;
0030 ;
0031 ;          PORTS USED BY DISK CONTROLLER
0032 ;
>0060        0033 X       EQU      60H
>0063        0034 SELECT  EQU      X+3      ; DRIVE SELECT PORT
>0064        0035 STATUS  EQU      X+4      ; STATUS PORT
>0065        0036 TRACK   EQU      X+5      ; TRACK PORT
>0066        0037 SECTOR  EQU      X+6      ; SECTOR PORT
>0067        0038 DATA   EQU      X+7      ; DATA PORT
>0064        0039 CMD     EQU      X+4      ; COMMAND PORT
0040 ;
0041 ;
0042 ;          SERIAL I/O PORTS
0043 ;
0044 ;
>007C        0045 SDATA   EQU      07CH      ; SERIAL DATA PORT
>007D        0046 SSTAT   EQU      07DH      ; SERIAL STATUS PORT
>0002        0047 RXRMSK  EQU      02H      ; RX RDY MASK
>0001        0048 TXRMSK  EQU      01H      ; TX RDY MASK
0049 ;
0050 ;
0051 ;          DISK ERROR STATUS BITS (ERSTAT)
0052 ;
0053 ;
0054 ;          BIT 7 - DRIVE NOT READY
0055 ;          BIT 6 - WRITE PROTECTED
0056 ;          BIT 5 - TRACK SEEK ERROR
0057 ;          BIT 4 - SECTOR NOT FOUND
0058 ;          BIT 3 - CRC ERROR
0059 ;          BIT 2 - DATA LOST

```

0060 ; BIT 1 - DRQ BIT
0061 ; BIT 0 - WRITE DELETED SECTOR READ
0062 ;
0063 ;
0064 ; DISK CONTROLLER COMMAND CODES
0065 ;
0066 ;
>00C4 0067 RDACMD EQU 0C4H ; READ ADDRESS CMD
>0088 0068 RDCMD EQU 88H ; READ SECTOR CMD
>00A8 0069 WRCMD EQU 0A8H ; WRITE SECTOR CMD
>00F4 0070 WRTCMD EQU 0F4H ; WRITE TRACK CMD
0071 ;
0072 ;

0074 ;
 0075 ; CP/M SYSTEM LINKAGES
 0076 ;
 0077 ;

F000	C349F0	0078	BIOS	JP	BOOT	; COLD START ENTRY
F003	C349F0	0079	WBOOT	JP	BOOT	; WARM START ENTRY
F006	C36AF0	0080	CSE	JP	CONST	; CONSOLE STATUS
F009	C372F0	0081	CIE	JP	CONIN	; READ CONSOLE
F00C	C37DF0	0082	COE	JP	CONOUT	; WRITE CONSOLE
F00F	C37DF0	0083	LSTE	JP	LIST	; WRITE PRINTER
F012	C37DF0	0084	PCHE	JP	PUNCH	; WRITE PUNCH
F015	C372F0	0085	RDRE	JP	READER	; READ READER
F018	C388F0	0086	HME	JP	HOME	; MOVE DISK TO TRK 00
F01B	C39AF0	0087	SDSKE	JP	SELDSK	; SELECT DISK DRIVE
F01E	C39FF0	0088	STRKE	JP	SETTRK	; SET DISK TRACK
F021	C3A4F0	0089	SSECE	JP	SETSEC	; SET DISK SECTOR
F024	C3A9F0	0090	SDMAE	JP	SETDMA	; SET MEM ADDR FOR READ/WRITE
F027	C3AFF0	0091	RDE	JP	READ	; READ A SECTOR
F02A	C3BEF0	0092	WRE	JP	WRITE	; WRITE A SECTOR
F02D	C354F2	0093	LDE	JP	LOADER	; LOAD 'N' SECTORS
F030	C361F2	0094	SVE	JP	SAVER	; SAVE 'N' RECORDS
F033	C330F3	0095	FMATE	JP	FMAT	; FORMAT A TRACK
F036	C30CF3	0096	SCANE	JP	SCAN	; SCAN FOR OPERAND
F039	C3AEF2	0097	PTXTE	JP	PTXT	; PRINT TEXT
F03C	C3BAF2	0098	PACCE	JP	PACC	; PRINT ACC
		0099				

```

0101 ;
0102 ;     MINI / FULL SIZE VARIABLES
0103 ;
0104 ;     SET UP THESE BYTES FOR THE TYPE OF
0105 ;     DRIVE TO BE USED.  THESE ARE THE ONLY
0106 ;     SOFTWARE CHANGES WITHIN BIOS TO CONVERT
0107 ;     FROM MINI TO FULL SIZE DRIVES (OR VISA
0108 ;     VERSA).
0109 ;
0110 ;
0111 ;
0112 ;
0113 NSCTRS  DEFB  12H  ; 12  1A  SCTRS/TRK
0114 NTRKS   DEFB  23H  ; 23  4D  TRACKS/SIDE
0115 GAP1    DEFB  14H  ; 14  4C  FORMAT GAP1
0116 GAP2    DEFB  11H  ; 11  11  FORMAT GAP2
0117 GAP3    DEFB  0EH  ; 0E  21  FORMAT GAP3
0118 RSCMD   DEFB  03H  ; 03  0A  RESTORE CMD
0119 SKCMD   DEFB  17H  ; 17  1E  SEEK CMD
0120 SKNCMD  DEFB  13H  ; 13  1A  SEEK W/NO VER
0121 HLDLY   DEFB  4BH  ; 4B  23  HEAD LOAD DELAY
0122 ;
0123 ;
0124 ;     DELAY CONSTANT MUST BE SET UP FOR
0125 ;     THE CPU CLOCK RATE USED:
0126 ;
0127 ;
0128 ;
0129 DLYCON   DEFB  8EH  ; 8E  B2  D8  00
  
```



```
F049 DB7F 0131 BOOT IN A, (07FH) ; CLEAR H. W.  
F04B 318000 0132 LD SP, SSTACK  
F04E 218000 0133 LD HL, COLD  
F051 224000 0134 LD (TADDR), HL  
F054 3E01 0135 LD A, 1  
F056 324500 0136 LD (NREC), A  
F059 324300 0137 LD (SCTR), A  
F05C AF 0138 XOR A  
F05D 324200 0139 LD (UNIT), A  
F060 324400 0140 LD (TRK), A  
F063 CD54F2 0141 CALL LOADER ; BOOT IN CP/M (EXCEPT CBIOS  
F066 CA8000 0142 JP Z, COLD ; JUMP TO COLD START  
F069 76 0143 HALT ; IF BAD DISK, HALT
```

```

0145 ;
0146 ; NON-DISK I/O DRIVER LINKAGES TO MOSTEK'S DDT
0147 ;
F06A DB7D 0148 CONST IN A, (SSTAT) ; CONSOLE STATUS
F06C E602 0149 AND RXRMSK
F06E C8 0150 RET Z
F06F 3EFF 0151 LD A, OFFH
F071 C9 0152 RET
0153 ;
0154 ; CONSOLE INPUT
0155 ;
F072 CD6AF0 0156 CONIN CALL CONST
F075 CA72F0 0157 JP Z, CONIN
F078 DB7C 0158 IN A, (SDATA)
F07A E67F 0159 AND 7FH
F07C C9 0160 RET
0161 ;
0162 ; CONSOLE OUTPUT
0163 ;
F07D DB7D 0164 CONOUT IN A, (SSTAT)
F07F E601 0165 AND TXRMSK ; TX BFR EMPTY
F081 CA7DF0 0166 JP Z, CONOUT
F084 79 0167 LD A, C
F085 D37C 0168 OUT (SDATA), A
F087 C9 0169 RET
0170 ;
0171 ; READER INPUT
0172 ;
>F072 0173 READER EQU CONIN
0174 ;
0175 ; LISTING OUTPUT
0176 ;
>F07D 0177 LIST EQU CONOUT
0178 ;
0179 ;
0180 ; PUNCH OUTPUT
0181 ;
>F07D 0182 PUNCH EQU CONOUT

```

```

    0184 ;
    0185 ;
    0186 ;
    0187 ;      DISK CONTROLLER LINKAGES
    0188 ;
    0189 ;
F088 CD3AF1 0190 HOME CALL   DRVSET ; SELECT DRIVE
F08B 210000 0191      LD     HL, 0
F08E 39      0192      ADD    HL, SP
F08F 224D00 0193      LD     (SPSV), HL
F092 3A44F0 0194      LD     A, (RSCMD)
F095 CDCCF1 0195      CALL  CMDI
F098 AF      0196      XOR    A
F099 C9      0197      RET
    0198 ;
    0199 ;      SELECT DISK DRIVE
    0200 ;
F09A 79      0201 SELDSK LD     A, C
F09B 324200 0202      LD     (UNIT), A
F09E C9      0203      RET
    0204 ;
    0205 ;      SET TRACK NUMBER
    0206 ;
F09F 79      0207 SETTRK LD     A, C
FOA0 324400 0208      LD     (TRK), A
FOA3 C9      0209      RET
    0210 ;
    0211 ;      SET SECTOR NUMBER
    0212 ;
FOA4 79      0213 SETSEC LD     A, C
FOA5 324300 0214      LD     (SCTR), A
FOA8 C9      0215      RET
    0216 ;
    0217 ;      SET MEMORY TRANSFER ADDRESS FOR DISK READ/WRITE
    0218 ;
FOA9 C5      0219 SETDMA PUSH   BC
FOAA E1      0220      POP    HL
FOAB 224000 0221      LD     (TADDR), HL
FOAE C9      0222      RET
    0223 ;
    0224 ;      READ A SECTOR
    0225 ;
FOAF 060A    0226 READ  LD     B, 10
FOB1 C5      0227 READ1 PUSH   BC
FOB2 CD6EF1 0228      CALL  RDSC ; READ A SECTOR
FOB5 C1      0229      POP    BC
FOB6 C8      0230      RET    Z ; RETURN IF NO ERROR
FOB7 05      0231      DEC    B
FOB8 C2B1F0 0232      JP     NZ, READ1 ; 10 RETRIES
FOBB AF      0233      XOR    A
FOBC 3C      0234      INC    A
FOBD C9      0235      RET ; ERROR RETURN
    0236 ;
    0237 ;      WRITE A SECTOR
    0238 ;
FOBE 060A    0239 WRITE LD     B, 10
FOCO C5      0240 WRITE1 PUSH   BC
  
```

FOC1	CD9DF1	0241	CALL	WRSC	; WRITE A SCTR
FOC4	C1	0242	POP	BC	
FOC5	C8	0243	RET	Z	; RETURN IF NO ERROR
FOC6	O5	0244	DEC	B	
FOC7	C2C0F0	0245	JP	NZ,WRITE1	
FOCA	AF	0246	XOR	A	
FOCB	3C	0247	INC	A	
FOCC	C9	0248	RET		; ERROR RETURN
		0249 ;			

```

0251 ;
0252 ;
0253 ;
0254 ; END OF COMMAND
0255 ;
0256 ;
0257 ;
FOCD DB64 0258 END IN A, ( STATUS )
FOCF E601 0259 AND 1
FOD1 C2CDF0 0260 JP NZ, END
FOD4 CDF0F1 0261 CALL DWAIT
FOD7 DB64 0262 IN A, ( STATUS )
FOD9 57 0263 LD D, A
FODA 3A4600 0264 LD A, ( ERMASK )
FODD A2 0265 AND D ; CHECK FOR ERRORS
FODE C8 0266 RET Z
FODF 7A 0267 END1 LD A, D
FOE0 324700 0268 END2 LD ( ERSTAT ), A ; SAVE ERROR BITS
FOE3 F601 0269 OR 1
FOE5 2A4D00 0270 LD HL, ( SPSV )
FOE8 F9 0271 LD SP, HL
FOE9 C9 0272 RET
0273 ;
0274 ;

```

```

0276 ;
0277 ;
0278 ; SELECT SIDE AND SEEK TRACK
0279 ;
FOEA 0600 0280 SEEK LD B,0
FOEC 3A40F0 0281 LD A,(NTRKS)
FOEF 4F 0282 LD C,A
FOFO 3A4400 0283 LD A,(TRK)
FOF3 B9 0284 CP C
FOF4 DAFAF0 0285 JP C,SEEK1
FOF7 0610 0286 LD B,10H ; SIDE 2
FOF9 91 0287 SUB C
FOFA 4F 0288 SEEK1 LD C,A ; SAVE NEW TRK #
FOFB DB65 0289 IN A,(TRACK) ; PRESENT TRACK
FOFD B9 0290 CP C
FOFE F5 0291 PUSH AF
FOFF DB63 0292 IN A,(SELECT)
F101 2F 0293 CPL
F102 5F 0294 LD E,A
F103 E610 0295 AND 10H ; CHECK SIDE SELECT
F105 B8 0296 CP B
F106 CA15F1 0297 JP Z,SEEK3 ; IF SAME SIDE, JUMP
F109 7B 0298 LD A,E
F10A E60F 0299 AND OFH
F10C B0 0300 OR B
F10D 2F 0301 CPL
F10E D363 0302 OUT (SELECT),A ; SELECT NEW SIDE
F110 3E01 0303 LD A,1
F112 CD26F2 0304 CALL MSEC
F115 F1 0305 SEEK3 POP AF
F116 C8 0306 RET ; IF SAME TRK, RETURN
F117 0603 0307 LD B,3 ; 3 RETRIES
F119 79 0308 SEEK2 LD A,C ; TRK #
F11A D367 0309 OUT (DATA),A
F11C 3A45F0 0310 LD A,(SKCMD) ; SEEK COMMAND
F11F C5 0311 PUSH BC ; SAVE RETRY COUNT AND TRK #
F120 CDCCF1 0312 CALL CMDI
F123 C1 0313 POP BC
F124 DB64 0314 IN A,(STATUS)
F126 E610 0315 AND 10H ; TEST FOR SEEK ERROR
F128 C8 0316 RET Z ; IF NO ERR, RET
F129 3A44F0 0317 LD A,(RSCMD)
F12C C5 0318 PUSH BC
F12D CDCCF1 0319 CALL CMDI ; RESTOR DISK
F130 C1 0320 POP BC
F131 05 0321 DEC B
F132 C219F1 0322 JP NZ,SEEK2
F135 3E20 0323 LD A,20H
F137 C3E0F0 0324 JP END2

```

```

0326 ;
0327 ;
0328 ; CHECK DRIVE SEL AND CHANGE IF DIFFERENT
0329 ;
0330 ;
F13A DB63 0331 DRVSET IN A,(SELECT)
F13C 2F 0332 CPL
F13D E60F 0333 AND OFH
F13F CA50F1 0334 JP Z,DRVS1 ; IF NONE, JUMP
F142 0EFF 0335 LD C,OFFH
F144 0C 0336 DRVSO INC C ; CONVERT TO DRV#
F145 1F 0337 RRA
F146 D244F1 0338 JP NC,DRVSO
F149 3A4200 0339 LD A,(UNIT)
F14C E603 0340 AND 3
F14E B9 0341 CP C
F14F C8 0342 RET Z ; IF SAME DRV, RETURN
F150 CDFF1 0343 DRVS1 CALL DRSEL
F153 AF 0344 XOR A
F154 3C 0345 INC A
F155 C9 0346 RET
0347 ;
0348 ;

```

ADDR	OBJECT	ST #	SOURCE STATEMENT
		0350	;
		0351	;
		0352	;
		0353	; READ PRESENT DISK ADDRESS (TRK &SCTR)
		0354	;
		0355	;
F156	214800	0356	IDRD LD HL, IDSV
F159	0604	0357	LD B, 4
F15B	3EF8	0358	LD A, 0F8H
F15D	324600	0359	LD (ERMASK), A
F160	CD7F1	0360	CALL SWEB
F163	3EC4	0361	LD A, RDACMD ; 'READ ADDRESS' CMD
F165	CD8BF1	0362	CALL RDSCO ; READ ID
F168	3A4800	0363	LD A, (IDSV)
F16B	D365	0364	OUT (TRACK), A
F16D	C9	0365	RET
		0366	;


```

0368 ;
0369 ;
0370 ; READ SECTOR COMMAND
0371 ;
0372 ;
F16E 210000 0373 RDSC LD HL, 0
F171 39 0374 ADD HL, SP
F172 224D00 0375 LD (SPSV), HL
F175 CD3AF1 0376 CALL DRVSET
F178 C456F1 0377 CALL NZ, IDR0 ; NEW DRIVE
F17B CDEAF0 0378 CALL SEEK ; SEEK TRACK
F17E 3EFE 0379 LD A, OFEH
F180 324600 0380 LD (ERMASK), A
F183 CD33F2 0381 CALL TRINT
F186 3E88 0382 LD A, RDCMD ; READ COMMAND
F188 CD40F2 0383 CALL HLCHK ; SET UP HEAD LOAD BIT
F18B 324C00 0384 RDSC0 LD (CMDSV), A
F18E D364 0385 OUT (CMD), A ; OUTPUT COMMAND
F190 DB67 0386 RDSC1 IN A, (DATA)
F192 77 0387 LD (HL), A
F193 23 0388 INC HL
F194 05 0389 DEC B
F195 C290F1 0390 JP NZ, RDSC1
F198 CDCDF0 0391 CALL END
F19B AF 0392 XOR A
F19C C9 0393 RET

```

ADDR	OBJECT	ST #	SOURCE STATEMENT
		0395 ;	
		0396 ;	
		0397 ;	WRITE SECTOR COMMAND
		0398 ;	
		0399 ;	
F19D	210000	0400	WRSC LD HL, 0
F1A0	39	0401	ADD HL, SP
F1A1	224D00	0402	LD (SPSV), HL
F1A4	CD3AF1	0403	CALL DRVSET
F1A7	C456F1	0404	CALL NZ, IDR0
F1AA	CDEAF0	0405	CALL SEEK
F1AD	3EFC	0406	LD A, OFCH
F1AF	324600	0407	LD (ERMASK), A
F1B2	CD33F2	0408	CALL TRINT
F1B5	3EA8	0409	LD A, WRCMD
F1B7	CD40F2	0410	CALL HLCHK
F1BA	324C00	0411	LD (CMDSV), A
F1BD	D364	0412	OUT (CMD), A ; OUTPUT COMMAND
F1BF	7E	0413	WRSC1 LD A, (HL)
F1C0	D367	0414	OUT (DATA), A
F1C2	23	0415	INC HL
F1C3	05	0416	DEC B
F1C4	C2BFF1	0417	JP NZ, WRSC1
F1C7	CDCDF0	0418	CALL END
F1CA	AF	0419	XOR A
F1CB	C9	0420	RET

```

0422 ;
0423 ;
0424 ;
0425 ; TYPE I COMMANDS
0426 ;
0427 ;
F1CC 324C00 0428 CMDI LD (CMDSV), A ; SAVE COMMAND
F1CF 3E80 0429 LD A, 080H
F1D1 324600 0430 LD (ERMASK), A
F1D4 DB64 0431 CMDI1 IN A, (STATUS)
F1D6 E601 0432 AND 1
F1D8 C2D4F1 0433 JP NZ, CMDI1 ; WAIT FOR NOT BUSY
F1DB DB63 0434 IN A, (SELECT)
F1DD E61F 0435 AND 1FH
F1DF F660 0436 OR 60H
F1E1 D363 0437 OUT (SELECT), A ; NO WAIT STATE ENBL
F1E3 3A4C00 0438 LD A, (CMDSV)
F1E6 D364 0439 OUT (CMD), A ; OUTPUT COMMAND
F1E8 3E01 0440 LD A, 1
F1EA CD26F2 0441 CALL MSEC ; WAIT FOR STATUS
F1ED C3CDF0 0442 JP END
0443 ;
0444 ;
0445 ;
0446 ;
0447 ;
0448 ; DISABLE WAIT STATES
0449 ;
F1F0 DB63 0450 DWAIT IN A, (SELECT)
F1F2 F6E0 0451 OR OEH ; NEG TRUE . AND.
F1F4 D363 0452 OUT (SELECT), A
F1F6 C9 0453 RET
0454 ;
0455 ;
0456 ; ENABLE WAIT STATES
0457 ;
0458 ;
F1F7 DB63 0459 SWEB IN A, (SELECT)
F1F9 E61F 0460 AND 1FH
F1FB D363 0461 OUT (SELECT), A
F1FD C9 0462 RET
0463 ;
0464 ;
0465 ; SELECT DRIVE
0466 ;
0467 ;
F1FE 3A4200 0468 DRSEL LD A, (UNIT)
F201 E603 0469 AND 3
F203 B7 0470 OR A ; CHECK FOR ZERO
F204 4F 0471 LD C, A
F205 3E01 0472 LD A, 1
F207 CA0FF2 0473 JP Z, DRSEL3 ; NO SHIFTING
F20A 07 0474 DRSEL2 RLCA ; SHIFT LEFT
F20B 0D 0475 DEC C
F20C C20AF2 0476 JP NZ, DRSEL2
F20F 2F 0477 DRSEL3 CPL
F210 D363 0478 OUT (SELECT), A

```

ADDR	OBJECT	ST #	SOURCE	STATEMENT
F212	3A47F0	0479	LD	A, (HL,DLY)
F215	CD26F2	0480	CALL	MSEC ; DELAY 35 MILLISECS
F218	DB64	0481	IN	A, (STATUS)
F21A	E680	0482	AND	80H
F21C	CA25F2	0483	JP	Z, DRSEL4
F21F	F1	0484	POP	AF
F220	3E40	0485	LD	A, 40H ; IF DRIVE NOT RDY, ERR
F222	C3E0F0	0486	JP	END2
F225	C9	0487	DRSEL4	RET
		0488		;
		0489		;
		0490		; DELAY (A REG) * 1 MILLISECOND
		0491		;
		0492		;
F226	47	0493	MSEC LD	B, A
F227	3A48F0	0494	MSECO LD	A, (DLYCON)
F22A	3D	0495	MSEC1 DEC	A
F22B	C22AF2	0496	JP	NZ, MSEC1
F22E	05	0497	DEC	B
F22F	C227F2	0498	JP	NZ, MSECO
F232	C9	0499	RET	
		0500		;
		0501		;
		0502		; INITIALIZE FOR DISK TRANSFER
		0503		;
		0504		;
F233	2A4000	0505	TRINT LD	HL, (TADDR)
F236	0680	0506	LD	B, NBYTES
F238	3A4300	0507	LD	A, (SCTR)
F23B	D366	0508	OUT	(SECTOR), A ; SELECT SECTORJ
F23D	C3F7F1	0509	JP	SWEB
		0510		;
		0511		;
		0512		;
		0513		; CHECK FOR HEAD LOADED, IF NOT SET
		0514		; 'H' BIT IN COMMAND.
		0515		;
		0516		;
F240	57	0517	HLCHK LD	D, A ; SAVE COMMAND IN D
F241	3ED0	0518	LD	A, ODOH
F243	D364	0519	OUT	(CMD), A ; 'FORCE INTERRUPT' CMD
F245	3E04	0520	LD	A, 4
F247	3D	0521	HLCHKO DEC	A
F248	C247F2	0522	JP	NZ, HLCHKO
F24B	DB64	0523	IN	A, (STATUS)
F24D	E620	0524	AND	20H
F24F	7A	0525	LD	A, D ; RESTORE COMMAND
F250	C0	0526	RET	NZ ; IF HEAD LOADED, RET
F251	F604	0527	OR	4 ; SET 'H' BIT
F253	C9	0528	RET	

ADDR	OBJECT	ST #	SOURCE	STATEMENT
		0530		;
		0531		;
		0532		LOAD # OF SECTORS IN (NREC)
		0533		;
		0534		;
F254	CDAFF0	0535	LOADER	CALL READ ; READ A SECTOR
F257	C28CF2	0536		JP NZ, ERR
F25A	CD6EF2	0537		CALL INCP ; INC TRK/SCTR
F25D	C254F2	0538		JP NZ, LOADER
F260	C9	0539		RET
		0540		;
		0541		;
		0542		;
		0543		;
		0544		SAVE # OF SECTORS IN (NREC)
		0545		;
		0546		;
F261	CDBEF0	0547	SAVER	CALL WRITE
F264	C28CF2	0548		JP NZ, ERR
F267	CD6EF2	0549		CALL INCP
F26A	C261F2	0550		JP NZ, SAVER
F26D	C9	0551		RET
		0552		;
		0553		INC SECTOR AND TRACK
		0554		;
		0555		;
F26E	2A4000	0556	INCP	LD HL, (TADDR)
F271	118000	0557		LD DE, NBYTES
F274	19	0558		ADD HL, DE
F275	224000	0559		LD (TADDR), HL
F278	214500	0560		LD HL, NREC ; POINT TO NREC
F27B	35	0561		DEC (HL)
F27C	C8	0562		RET Z
F27D	2B	0563		DEC HL
F27E	2B	0564		DEC HL ; POINT TO SCTR
F27F	34	0565		INC (HL) ; INC SCTR #
F280	3A3FF0	0566		LD A, (NSCTRS)
F283	3C	0567		INC A
F284	BE	0568		CP (HL) ; LAST SCTR ON TRK ?
F285	C0	0569		RET NZ ; IF NOT, RETURN
F286	3601	0570		LD (HL), 1 ; SET TO SCTR 1
F288	23	0571		INC HL ; POINT TO TRK
F289	34	0572		INC (HL) ; INC TRK #
F28A	B7	0573		OR A
F28B	C9	0574		RET
		0575		;
		0576		;
		0577		ERROR MESSAGE 'DISK ERR#'
		0578		;
		0579		;
F28C	21A3F2	0580	ERR	LD HL, ERMSG
F28F	CDAEF2	0581		CALL PTXT
F292	3A4700	0582		LD A, (ERSTAT)
F295	CDBAF2	0583		CALL PACC
F298	OE0A	0584		LD C, OAH
F29A	CD7DF0	0585		CALL CONOUT
F29D	OE0D	0586		LD C, ODH

ADDR	OBJECT	ST #	SOURCE STATEMENT		
F29F	C37DF0	0587		JP	CONOUT
F2A2	C9	0588		RET	
		0589 ;			
F2A3	4449534B	0590	ERMSG	DEFM	'DISK ERR# '
	20455252				
	2320				
F2AD	03	0591		DEFB	3
		0592 ;			
		0593 ;			
		0594 ;	PRINT TEXT		
		0595 ;			
		0596 ;			
F2AE	7E	0597	PTXT	LD	A, (HL) ; FETCH A BYTE
F2AF	FE03	0598		CP	3
F2B1	C8	0599		RET	Z
F2B2	4F	0600		LD	C, A
F2B3	CD7DF0	0601		CALL	CONOUT
F2B6	23	0602		INC	HL
F2B7	C3AEF2	0603		JP	PTXT
		0604 ;			
		0605 ;			
		0606 ;	PRINT ACCUMULATOR		
		0607 ;			
		0608 ;			
F2BA	F5	0609	PACC	PUSH	AF
F2BB	0F	0610		RRCA	
F2BC	0F	0611		RRCA	
F2BD	0F	0612		RRCA	
F2BE	0F	0613		RRCA	
F2BF	CDC3F2	0614		CALL	PRVAL
F2C2	F1	0615		POP	AF
		0616 ;			
		0617 ;			
F2C3	E60F	0618	PRVAL	AND	0FH
F2C5	C690	0619		ADD	A, 90H
F2C7	27	0620		DAA	
F2C8	CE40	0621		ADC	A, 40H
F2CA	27	0622		DAA	
F2CB	4F	0623		LD	C, A
F2CC	C37DF0	0624		JP	CONOUT ; PRINT IT
		0625 ;			
		0626 ;			
		0627 ;	ASCII TO BINARY CONVERSION		
		0628 ;			
		0629 ;			
F2CF	D630	0630	ASBIN	SUB	30H
F2D1	FE0A	0631		CP	10
F2D3	F8	0632		RET	M
F2D4	D607	0633		SUB	7
F2D6	C9	0634		RET	
		0635 ;			
		0636 ;			
		0637 ;	CHECK FOR VALID HEX CHARACTER		
		0638 ;			
		0639 ;			
F2D7	FE30	0640	AORN	CP	'0'
F2D9	DAEDF2	0641		JP	C, AORN2 ; JUMP IF < 30H
F2DC	FE3A	0642		CP	'9'+1

ADDR	OBJECT	ST #	SOURCE	STATEMENT
F2DE	DAEBF2	0643		JP C,AORN1 ; JUMP IF < 3AH
F2E1	FE40	0644		CP 'A'-1
F2E3	DAEDF2	0645		JP C,AORN2 ; JUMP IF < 'A'
F2E6	FE47	0646		CP 'F'+1
F2E8	D2EDF2	0647		JP NC,AORN2 ; JUMP IF < 'G'
F2EB	AF	0648	AORN1	XOR A
F2EC	C9	0649		RET ; VALID DATA RET
F2ED	AF	0650	AORN2	XOR A
F2EE	3C	0651		INC A
F2EF	C9	0652		RET ; NOT HEX CHAR
		0653		;
		0654		;
		0655		; CHECK FOR TERMINATOR
		0656		;
		0657		; SPACE, COMMA, OR CARRIAGE RETURN
		0658		;
		0659		;
F2F0	FE20	0660	TERMCK	CP / /
F2F2	C8	0661		RET Z
F2F3	FE2C	0662		CP ', '
F2F5	C8	0663		RET Z
F2F6	FE5E	0664		CP '^ ^'
F2F8	CA03F3	0665		JP Z,TCHKO
F2FB	FE2E	0666		CP ' ' /
F2FD	CA03F3	0667		JP Z,TCHKO
F300	FE0D	0668		CP ODH
F302	C0	0669		RET NZ
F303	C5	0670	TCHKO	PUSH BC
F304	OE0A	0671		LD C,OAH
F306	CD7DF0	0672		CALL CONOUT
F309	C1	0673		POP BC
F30A	AF	0674		XOR A
F30B	C9	0675		RET
		0676		;
		0677		;
		0678		; SCAN FOR OPERAND FROM KEYBOARD
		0679		;
		0680		;
		0681		; EXIT WITH DATA IN HL, AND TERMINATOR
		0682		; IN C. IF VALID DATA, RETURN WITH
		0683		; ZERO FLAG SET. B CONTAINS # OF CHARACTERS ENTERED.
		0684		;
		0685		;
F30C	210000	0686	SCAN	LD HL,0
F30F	45	0687		LD B,L
F310	CD29F3	0688	SCAN1	CALL ECHO
F313	04	0689		INC B ; INC CHAR COUNT
F314	CDF0F2	0690		CALL TERMCK
F317	C8	0691		RET Z ; IF TERMINATOR, RETURN
F318	CDD7F2	0692		CALL AORN ; VALID DATA CHECK
F31B	C0	0693		RET NZ ; IF NOT RETURN
F31C	79	0694		LD A,C
F31D	CDCFF2	0695		CALL ASBIN ; CONVERT TO BINARY
F320	29	0696		ADD HL,HL
F321	29	0697		ADD HL,HL
F322	29	0698		ADD HL,HL
F323	29	0699		ADD HL,HL ; P SHIFT 4 BITS
F324	85	0700		ADD A,L

ADDR OBJECT ST # SOURCE STATEMENT

F325	6F	0701	LD	L, A
F326	C310F3	0702	JP	SCAN1
		0703 ;		
		0704 ;		
		0705 ;		
F329	CD72F0	0706 ECHO	CALL	CONIN
F32C	4F	0707	LD	C, A
F32D	C37DF0	0708	JP	CONOUT


```

0710 ;
0711 ;
0712 ;
0713 ; FORMAT A TRACK ( IBM MINI DISK FORMAT )
0714 ;
0715 ;
F330 3A4400 0716 FMAT LD A, ( TRK )
F333 D367 0717 OUT ( DATA ), A
F335 3A46F0 0718 LD A, ( SKNCMD )
F338 CDCCF1 0719 CALL CMDI
F33B 2E01 0720 LD L, 1
F33D 3A3FF0 0721 LD A, ( NSCTRS )
F340 67 0722 LD H, A
F341 3A41F0 0723 LD A, ( GAP1 )
F344 47 0724 LD B, A
F345 AF 0725 XOR A
F346 324600 0726 LD ( ERMASK ), A
F349 CDF7F1 0727 CALL SWEB
F34C 3EF4 0728 LD A, WRTCMD
F34E 324C00 0729 LD ( CMDSV ), A
F351 D364 0730 OUT ( CMD ), A ; OUTPUT COMMAND
F353 AF 0731 XOR A
F354 D367 0732 FMAT3 OUT ( DATA ), A ; GAP1
F356 05 0733 DEC B
F357 C254F3 0734 JP NZ, FMAT3
F35A 3EFE 0735 FMAT5 LD A, OFEH ; ID ADDRESS MARK
F35C D367 0736 OUT ( DATA ), A
F35E DB65 0737 IN A, ( TRACK )
F360 D367 0738 OUT ( DATA ), A ; TRACK #
F362 AF 0739 XOR A
F363 D367 0740 OUT ( DATA ), A ; 0 GAP
F365 7D 0741 LD A, L
F366 D367 0742 OUT ( DATA ), A ; SECTOR #
F368 AF 0743 XOR A
F369 D367 0744 OUT ( DATA ), A ; SECTOR LENGTH = 128
F36B 3EF7 0745 LD A, OF7H ; SEND CRC ( 2 BYTES )
F36D D367 0746 OUT ( DATA ), A
F36F 3A42F0 0747 LD A, ( GAP2 )
F372 47 0748 LD B, A
F373 AF 0749 XOR A
F374 D367 0750 FMAT6 OUT ( DATA ), A ; GAP2
F376 05 0751 DEC B
F377 C274F3 0752 JP NZ, FMAT6
F37A 3EFB 0753 LD A, OFBH ; DATA ADDRESS MARK
F37C D367 0754 OUT ( DATA ), A
F37E 3EE5 0755 LD A, OE5H
F380 0680 0756 LD B, 128D
F382 D367 0757 FMAT7 OUT ( DATA ), A ; 128 E5'S IN DATA FIELD
F384 05 0758 DEC B
F385 C282F3 0759 JP NZ, FMAT7
F388 3EF7 0760 LD A, OF7H
F38A D367 0761 OUT ( DATA ), A ; CRC ( 2 BYTES )
F38C 3A43F0 0762 LD A, ( GAP3 )
F38F 47 0763 LD B, A
F390 AF 0764 XOR A
F391 D367 0765 FMAT8 OUT ( DATA ), A ; GAP3
F393 05 0766 DEC B

```

F394	C291F3	0767	JP	NZ,FMAT8	
F397	2C	0768	INC	L	; INC SECTOR #
F398	25	0769	DEC	H	; CHECK FOR LAST SECTOR
F399	C25AF3	0770	JP	NZ,FMAT5	; WRITE ALL SECTORS
F39C	CDCDF0	0771	CALL	END	
F39F	AF	0772	XOR	A	
F3A0	C9	0773	RET		

APPENDIX E
VERSAFLOPPY DIAGNOSTIC
SOFTWARE

```

0002      NAME      VDIAG
0003 ;
0004 ;      VERSION 1.0      3/17/78
0005 ;      RUNS ON Z80, 8080, AND 8085
0006 ;
0007      PSECT     ABS
>0100    0008      ORG      100H
0009 ;
0010 ;      BIOS LINKAGES
0011 ;
>F000    0012 BIOS     EQU      0F000H
>F006    0013 CSE     EQU      BIOS+6
>F009    0014 CIE     EQU      BIOS+9
>F00C    0015 COE     EQU      BIOS+0CH
>F018    0016 HME     EQU      BIOS+18H
>F027    0017 RDE     EQU      BIOS+27H
>F02A    0018 WRE     EQU      BIOS+2AH
>F02D    0019 LDE     EQU      BIOS+2DH
>F030    0020 SVE     EQU      BIOS+30H
>F033    0021 FMATE   EQU      BIOS+33H
>F036    0022 SCANE   EQU      BIOS+36H
>F039    0023 PTXTE   EQU      BIOS+39H
>F03C    0024 PACCE   EQU      BIOS+3CH
>F03F    0025 NSCTRS  EQU      BIOS+3FH
>F040    0026 NTRKS   EQU      BIOS+40H
>F046    0027 SKNCMD  EQU      BIOS+46H
0028 ;
>0000    0029 RBASE   EQU      0000H ; RAM START
>0040    0030 TADDR   EQU      RBASE+40H
>0042    0031 UNIT    EQU      RBASE+42H
>0043    0032 SCTR    EQU      RBASE+43H
>0044    0033 TRK     EQU      RBASE+44H
>0045    0034 NREC    EQU      RBASE+45H
>0046    0035 ERMASK  EQU      RBASE+46H
>0047    0036 ERSTAT  EQU      RBASE+47H
>0048    0037 IDSV    EQU      RBASE+48H
>004C    0038 CMDSV   EQU      RBASE+4CH
>0039    0039 RQST    EQU      RBASE+39H
>0038    0040 RANDB   EQU      RBASE+38H
>003A    0041 NUMB    EQU      RBASE+3AH
0042 ;
0043 ;
>0800    0044 BFFR1   EQU      RBASE+800H
>0880    0045 BFFR2   EQU      RBASE+880H
>0080    0046 USRSP   EQU      RBASE+80H
>0080    0047 NBYTES  EQU      128
0048 ;
0049 ;
>0060    0050 X        EQU      60H
>0064    0051 STATUS  EQU      X+4
>0064    0052 CMD      EQU      X+4
>0067    0053 DATA   EQU      X+7

```

```

0055 ;
0056 ;
0057 ;
0058 ;
0059 ; DISK DRIVE EVALUATION EXEC
0060 ;
0061 ;
0100 318000 0062 DEXEC LD SP,USRSP
0103 213101 0063 LD HL,MSG1
0106 CD39F0 0064 CALL PTXTE ; "ENTER REQUEST #, DRIVE # "
0109 CD36F0 0065 CALL SCANE
010C C22601 0066 JP NZ,INERR
010F 7D 0067 LD A,L
0110 324200 0068 LD (UNIT),A
0113 7C 0069 LD A,H
0114 323900 0070 LD (RQST),A
0117 CD5001 0071 CALL DECODE ; DECODE AND EXECUTE CMD
011A CD18F0 0072 CALL HME
011D 214401 0073 LD HL,MSG3
0120 CD39F0 0074 CALL PTXTE ; "TASK COMPLETE"
0123 C30001 0075 JP DEXEC
0076 ;
0126 0E3F 0077 INERR LD C,'?'
0128 CD0CF0 0078 CALL COE
012B CD3103 0079 CALL CRLF
012E C30001 0080 JP DEXEC
0081 ;
0131 54455354 0082 MSG1 DEFM 'TEST#DRV# (TTDD): '
23445256
23202854
54444429
3A20
0143 03 0083 DEFB 03
0144 5441534B 0084 MSG3 DEFM 'TASK DONE'
20444F4E
45
014D 0DOA 0085 DEFW 0A0DH
014F 03 0086 DEFB 03

```

```

0088 ;
0089 ;
0090 ; DECODE REQUEST AND EXECUTE IT
0091 ;
0150 FE00      0092 DECODE  CP      0
0152 CA1403   0093      JP      Z, TSTSK ; SEEK TEST
0155 FE01     0094      CP      1
0157 CAFC01   0095      JP      Z, DIAG
015A FE02     0096      CP      2
015C CAFC01   0097      JP      Z, DIAG
015F FE03     0098      CP      3
0161 CAFC01   0099      JP      Z, DIAG
0164 FE04     0100      CP      4
0166 CAFC01   0101      JP      Z, DIAG
0169 FE05     0102      CP      5
016B CA8F01   0103      JP      Z, FORMT
016E FE10     0104      CP     10H
0170 CA4003   0105      JP      Z, LOAD
0173 FE11     0106      CP     11H
0175 CA5B03   0107      JP      Z, SAVE
0178 FEFF     0108      CP     OFFH
017A C0       0109      RET     NZ
017B 218501   0110      LD     HL, MSG2
017E CD39F0   0111      CALL  PTXTE
0181 CD36F0   0112      CALL  SCANE
0184 E9       0113      JP     (HL)
0114 ;
0115 ;
0185 41444452 0116 MSG2   DEFM   'ADDRESS:
      4553533A
      20
018E 03       0117      DEFB   3
  
```

```

0119 ;
0120 ; FORMAT A DISKETTE
0121 ;
0122 ;
018F AF      0123 FORMT   XOR      A
0190 324400 0124        LD      (TRK),A
0193 3C      0125        INC     A
0194 324300 0126        LD      (SCTR),A
0197 CD18F0 0127        CALL   HME
019A CD33F0 0128 FORMT1  CALL   FMATE
019D C2B001 0129        JP      NZ,ERROR
01A0 3A4400 0130        LD      A,(TRK)
01A3 3C      0131        INC     A
01A4 324400 0132        LD      (TRK),A
01A7 47      0133        LD      B,A
01A8 3A40F0 0134        LD      A,(NTRKS)
01AB B8      0135        CP      B
01AC C29A01 0136        JP      NZ,FORMT1
01AF C9      0137        RET
0138 ;
0139 ;
0140 ;
0141 ;
0142 ; ERROR PRINT ROUTINE
0143 ;
0144 ;
01B0 21E401 0145 ERROR   LD      HL,ERMSG
01B3 CD39F0 0146        CALL   PTXTE ; "DISK ERROR ..."
01B6 3A4C00 0147        LD      A,(CMDSV)
01B9 CD3CF0 0148        CALL   PACCE ; PRINT COMMAND
01BC CD3B03 0149        CALL   SPACE
01BF 3A4700 0150        LD      A,(ERSTAT)
01C2 CD3CF0 0151        CALL   PACCE ; PRINT STATUS
01C5 CD3B03 0152        CALL   SPACE
01C8 3A4200 0153        LD      A,(UNIT)
01CB CD3CF0 0154        CALL   PACCE ; UNIT #
01CE CD3B03 0155        CALL   SPACE
01D1 3A4400 0156        LD      A,(TRK)
01D4 CD3CF0 0157        CALL   PACCE
01D7 CD3B03 0158        CALL   SPACE
01DA 3A4300 0159        LD      A,(SCTR)
01DD CD3CF0 0160        CALL   PACCE
01E0 CD3103 0161        CALL   CRLF
01E3 C9      0162        RET
0163 ;
0164 ;
01E4 434D4420 0165 ERMSG   DEFB   <CMD STAT DRV TRK SCTR>
53544154
20445256
2054524B
20534354
523E20
01FB 03      0166        DEFB   03
0167 ;
0168 ;
0169 ;
0170 ; READ / WRITE DIAGNOSTIC

```

0171 ; CONTINUES UNTIL A ' ' IS ENTERED FROM KEYBOARD

0172 ;

0173 ;

0174 ;

01FC	AF	0175	DIAG	XOR	A
01FD	324400	0176		LD	(TRK), A
0200	3C	0177		INC	A
0201	324300	0178		LD	(SCTR), A
0204	C35202	0179		JP	DIAG1
0207	210008	0180	DIA10	LD	HL, BFFR1
020A	224000	0181		LD	(TADDR), HL
020D	CD2AF0	0182		CALL	WRE
0210	C4B001	0183		CALL	NZ, ERROR
0213	218008	0184	DIA11	LD	HL, BFFR2
0216	224000	0185		LD	(TADDR), HL
0219	CD27F0	0186		CALL	RDE
021C	C4B001	0187		CALL	NZ, ERROR
021F	3A3900	0188		LD	A, (RQST)
0222	FE02	0189		CP	2
0224	CA3402	0190		JP	Z, DIAG3
0227	FE03	0191		CP	3
0229	CACA02	0192		JP	Z, RINCR
022C	FE04	0193		CP	4
022E	CABB02	0194		JP	Z, DINCR
0231	CD7302	0195		CALL	COMPR ; IF DIAG 1, COMPARE
0234	214300	0196	DIAG3	LD	HL, SCTR
0237	34	0197		INC	(HL) ; INC SECTOR
0238	3A3FF0	0198		LD	A, (NSCTRS)
023B	3C	0199		INC	A
023C	BE	0200		CP	(HL)
023D	C25202	0201		JP	NZ, DIAG1 ; IF NOT END OF TRK, JMP
0240	3601	0202		LD	(HL), 1 ; SET TO SCTR 1
0242	23	0203		INC	HL ; POINT TO TRK
0243	34	0204		INC	(HL) ; INC TRK #
0244	3A40F0	0205	DIAG4	LD	A, (NTRKS)
0247	BE	0206		CP	(HL)
0248	C25202	0207		JP	NZ, DIAG1
024B	3600	0208		LD	(HL), 0 ; SET TO TRK 00
024D	0E50	0209		LD	C, 'P'
024F	CD0CF0	0210		CALL	COE ; PRINT 'P' EVERY COMPLETE PASS
0252	CD06F0	0211	DIAG1	CALL	CSE
0255	CA5E02	0212		JP	Z, DIAG2
0258	CD09F0	0213		CALL	CIE
025B	FE2E	0214		CP	' '
025D	C8	0215		RET	Z
025E	3A3900	0216	DIAG2	LD	A, (RQST)
0261	FE02	0217		CP	2
0263	CA1302	0218		JP	Z, DIA11
0266	FE01	0219		CP	1
0268	CA0702	0220		JP	Z, DIA10
026B	FE03	0221		CP	3
026D	CA0702	0222		JP	Z, DIA10
0270	C30702	0223		JP	DIA10
		0224			;
		0225			;
		0226			;
0273	210008	0227	COMPR	LD	HL, BFFR1
0276	118008	0228		LD	DE, BFFR2

ADDR	OBJECT	ST #	SOURCE	STATEMENT
0279	0680	0229		LD B, NBYTES
027B	1A	0230	CMPR1	LD A, (DE)
027C	BE	0231		CP (HL)
027D	3FFF	0232		LD A, OFFH
027F	324700	0233		LD (ERSTAT), A
0282	C2B001	0234		JP NZ, ERROR
0285	23	0235		INC HL
0286	13	0236		INC DE
0287	05	0237		DEC B
0288	C27B02	0238		JP NZ, CMPR1
028B	CD8F02	0239		CALL INCRD
028E	C9	0240		RET
		0241 ;		
		0242 ;		
		0243 ;		
		0244 ;		
		0245 ;		
		0246 ;		
		0247 ;		
028F	110008	0248	INCRD	LD DE, BFFR1
0292	0640	0249		LD B, NBYTES/2
0294	3A3800	0250		LD A, (RANDS)
0297	FE01	0251		CP 1
0299	CA9D02	0252		JP Z, HERE
029C	13	0253		INC DE
029D	CD502	0254	HERE	CALL PRAND
02A0	12	0255		LD (DE), A
02A1	13	0256		INC DE
02A2	13	0257		INC DE
02A3	05	0258		DEC B
02A4	C29D02	0259		JP NZ, HERE
02A7	3A3800	0260		LD A, (RANDS)
02AA	FE01	0261		CP 1
02AC	CAB502	0262		JP Z, SKIP
02AF	3E01	0263		LD A, 1
02B1	323800	0264		LD (RANDS), A
02B4	C9	0265		RET
02B5	3E00	0266	SKIP	LD A, 0
02B7	323800	0267		LD (RANDS), A
02BA	C9	0268		RET
		0269 ;		
		0270 ;		
		0271 ;		
02BB	CD7302	0272	DINCR	CALL COMPR
02BE	CD502	0273		CALL PRAND
02C1	34	0274		INC (HL) ; INC SEED
02C2	E601	0275		AND 1
02C4	324200	0276		LD (UNIT), A ; RANDOM UNIT
02C7	C3CD02	0277		JP RINCR1
02CA	CD7302	0278	RINCR	CALL COMPR
02CD	3A3FF0	0279	RINCR1	LD A, (NSCTRS)
02D0	3C	0280		INC A
02D1	47	0281		LD B, A
02D2	CD502	0282		CALL PRAND
02D5	E61F	0283		AND 01FH
02D7	B7	0284		OR A
02D8	CACD02	0285		JP Z, RINCR1 ; SECTOR 0 ILLEGA
02DB	324300	0286		LD (SCTR), A

```

02DE B8          0287          CP          B
02DF D2CD02      0288          JP          NC, RINCR1      ; IF NO>NSCTRS TRY AGAIN
02E2 3A40F0     0289 ONCM        LD          A, ( NTRKS )
02E5 47         0290          LD          B, A
02E6 CDF502     0291          CALL       PRAND
02E9 E67F       0292          AND        07FH
02EB 324400     0293          LD          ( TRK ), A
02EE B8         0294          CP          B
02EF D2E202     0295          JP          NC, ONCM      ; IF NO>NTRKS TRY AGAIN
02F2 C35202     0296          JP          DIAG1
                0297 ;
                0298 ;
                0299 ;
                0300 ;          PSEUDO RANDOM NUMBER GENERATOR
                0301 ;
                0302 ;
02F5 D5         0303 PRAND      PUSH       DE
02F6 C5         0304          PUSH      BC
02F7 213A00     0305          LD        HL, NUMB ; LOCATION OF SEED
02FA 0E00      0306          LD        C, 0
02FC 7E        0307          LD        A, ( HL )
02FD A7         0308          AND      A
02FE C20303     0309          JP        NZ, NEXT
0301 3EFF      0310          LD        A, OFFH
0303 57        0311 NEXT     LD        D, A
0304 E61D      0312          AND      1DH
0306 EA0B03     0313          JP        PE, PAR
0309 0E80      0314          LD        C, 80H
030B 7A       0315 PAR     LD        A, D
030C 0F        0316          RRCA
030D E67F     0317          AND      7FH
030F 81       0318          ADD     A, C
0310 77       0319          LD        ( HL ), A
0311 C1       0320          POP     BC
0312 D1       0321          POP     DE
0313 C9       0322          RET
                0323 ;
                0324 ;
                0325 ;
                0326 ;
0314 CD18F0     0327 TSTSK   CALL     HME
0317 3A40F0     0328          LD        A, ( NTRKS )
031A 3D        0329          DEC     A
031B D367      0330          OUT     ( DATA ), A
031D 3A46F0     0331          LD        A, ( SKNCMD ) ; SEEK ( NO VERIFY )
0320 D364      0332          OUT     ( CMD ), A
0322 CD06F0     0333          CALL    CSE
0325 CA1403     0334          JP        Z, TSTSK
0328 CD09F0     0335          CALL    CIE
032B FE2E     0336          CP
032D C8        0337          RET     Z
032E C31403     0338          JP        TSTSK
                0339 ;
                0340 ;
                0341 ;
                0342 ;
0331 0E0D      0343 CRLF    LD        C, 0DH
0333 CD0CF0     0344          CALL    COE

```

0336	0E0A	0345	LD	C, OAH
0338	030CF0	0346	JP	COE
		0347 ;		
		0348 ;		
033B	0E20	0349 SPACE	LD	C, / /
033D	030CF0	0350	JP	COE
		0351 ;		
		0352 ;		

```

0354 ;
0355 ;
0356 ;
0357 ;      LOAD 'N' SECTORS
0358 ;
0359 ;
0340 214903 0360 LOAD   LD      HL, LDMSG
0343 CD7603 0361      CALL   STUFF
0346 C32DF0 0362      JP      LDE
0363 ;
0349 454E5445 0364 LDMSG  DEFM   'ENTER LOAD ADDR: '
52204C4F
41442041
4444523A
20
035A 03      0365      DEFB   3
0366 ;
0367 ;
0368 ;
0369 ;      SAVE 'N' SECTORS
0370 ;
0371 ;
035B 216403 0372 SAVE   LD      HL, SVMSG
035E CD7603 0373      CALL   STUFF
0361 C330F0 0374      JP      SVE
0375 ;
0364 454E5445 0376 SVMSG  DEFM   'ENTER SAVE ADDR: '
52205341
56452041
4444523A
20
0375 03      0377      DEFB   3
0378 ;
0379 ;
0380 ;
0381 ;      STUFF DISK PARAMS
0382 ;
0383 ;
0384 ;
0376 CD39F0 0385 STUFF  CALL   PTXTE
0379 CD36F0 0386      CALL   SCANE
037C C22601 0387      JP      NZ, INERR
037F 224000 0388      LD      ( TADDR ), HL
0382 21A203 0389      LD      HL, TSMSG
0385 CD39F0 0390      CALL   PTXTE
0388 CD36F0 0391      CALL   SCANE
038B C22601 0392      JP      NZ, INERR
038E 224300 0393      LD      ( SCTR ), HL      ; SECTOR & TRACK
0391 21BE03 0394      LD      HL, SZMSG
0394 CD39F0 0395      CALL   PTXTE
0397 CD36F0 0396      CALL   SCANE
039A C22601 0397      JP      NZ, INERR
039D 7D      0398      LD      A, L
039E 324500 0399      LD      ( NREC ), A      ; # OF SECTORS
03A1 C9      0400      RET
0401 ;
03A2 454E5445 0402 TSMSG  DEFM   'ENTER TRACK/SECTOR ( TTSS ): '

```

VDIAG COPYRIGHT 1978 SD SALES COMPANY MOSTEK FLP-80 ASSEMBLER V1.0 PAGE 0010
ADDR OBJECT ST # SOURCE STATEMENT

52205452
41434B2F
53454354
4F522028
54545353
293A20
03BD 03 0403 DEFB 3
03BE 454E5445 0404 SZMSG DEFM 'ENTER NUMBER OF SECTORS (NN):'
52204E55
4D424552
204F4620
53454354
4F525320
284E4E29
3A
03DB 03 0405 DEFB 3