TABLE OF CONTENTS

Teletek 1981
Revision 2

S-100 Bus Interface

Signal Used	Description
PHANTOM*	Disable signal to slaves
RDY	Ready input to bus master
0	Master timing signal
pSTVAL*	Status valid strobe
RESET*	System reset signal
pSYNC	New bus cycle signal
pWR*	Write strobe
pDBIN	Read strobe
A0-A15	16-bit address bus
D00-D07	8-bit data out bus
DI0-DI7	8-bit data in bus
sM1	Op-code fetch status signal
sOUT	Output status signal
sINP	Input status signal
sINTA	Interrupt acknowledge status signal
sMEMR	Memory read status signal
sWO*	Write cycle status signal
CLOCK	2 MHz clock
+8	
+16	
-16	
GND	

MEMORY BOARD SETUP

CPU Timing

Jumper area A, located between U-1 and U-2, determines the time when a refresh cycle is started. For most Z-80 boards, including Teletek's FDC-I, jumper the center post to the bottom post. This enables the refresh cycle from a delayed sM1. Optionally, the center post can be jumpered to the top post which ANDs pSTVAL and pDBIN for most 8080 boards or to the right post which provides a delayed sM1.

Jumper area B, located below U-3, along with jumper area C, between U-20 and U-21, set up the timing for the start of a memory cycle. For the FDC-I and most other Z-80 CPU boards jumper the center post in area B to the left post (delayed sM1) and the center post in area C to the top post. Options for area B are the right post (sM1) for Z-80's and the bottom post (OR of sWO* and delayed sM1) for 8080 CPU's.

Jumper are D, located between U-3 and U-4, is used only when jumper area A has been selected for 8080 or Alpha Micro CPU's. Jumper area D allows the option of selectin 0 (bottom post) or pSTVAL* (top post) as the signal that is ANDed with pDBIN to determine when a refresh is started.

Jumper area E, located between U-4 and U-5, allows the selection of sM1 (top post) or pSYNC (bottom post) as the signal to start a memory cycle. For most Z-80's and the FDC-I sM1 is used. For 8080 CPu's pSYNC is used.

Jumper area F, located between U-5 and U-12, determines the signal used to start a memory read cycle. For most 8080 CPU's and the FDC-I use pDBIN (right post). For most Z-80's use sMEMR (left post).

Bank Select 64K Version

The Teletek 64K memory board supports either the Cromemco/Alpha Micro or the North Star methods for bank selection.

There are four banks of 16K bytes each. Each bank can be addressed starting at 0000H, 4000H, 8000H, or C000H. Each bank can be turned on or off during a system reset. Each bank can respond to the PHANTOM* disable signal if desired. In addition, there is provided the ability to deselect memory either above or below any address chosen on a 4K boundary.

U-13 is a 16-pin header allowing the configuration of the bank selection method. The following is a list of the signal names on the header.

U-31

Header

Pin	Signal Name
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	AEN
10	DD
11	BEN
12	CD
13	CEN
14	BD
15	DEN
16	AD

In the North Star bank select scheme the four signals AD, BD, CD and DD connect to DO. The user then has the option of defining seven banks using bits D1-D7 connected appropriately to AEN-DEN. The signals AEN-DEN disable the ability to change the status of the four banks on any particular memory board. This method requires two I/O output instructions in order to turn banks on and off.

The Cromemco/Alpha Micro bank select scheme requires only one I/O output instruction to have the same effect. In this scheme the AEN-DEN signals are not used. Instead, AD-DD are connected appropriately to DO-D7 to allow eight possible banks of memory.

Bank Enable/Disable on RESET

The four banks can be enabled or disabled on system RESET at the user's option. Four sets of jumpers are located between U-23 and U-24 (banks A and B) and also between U-16 and U-17 (banks C and D). Each set consists of a center post and a clear post above and a preset post below. In order to enable a bank on reset, connect the center post for a given bank (A-D) to the post below (preset).

Bank Addressing

The four banks can be addressed on any 16k boundary. There are two jumpers for each bank that determine the address for that bank. The jumpers for banks A and B are located below U-7. The jumpers for banks C and D are located below U-6.

To address a bank at 0000H remove both jumpers for that bank; for 4000H install the left jumper only; for 8000H install the right jumper only. For the bank to be addressed at C000H install both left and right jumpers for that bank.

Phantom

Between the two sets of jumpers for bank addressing are the jumpers for PHANTOM* disable. Any bank may be disabled by the PHANTOM* signal at the user's option. There are three posts for each bank and a center post that is jumpered either to PHANTOM* signal. The two posts on the left side and the two posts on the right side are grounded. Therefore, to disable bank A on PHANTOM connect the center post for bank A to the post on the left. In the same manner, to disable bank D on PHANTOM* connect the center post for bank D to the post on the right. If PHANTOM* is not used, connect all four jumpers to ground.

4K Block Deselect

The memory board has the option for deselecting a block of memory above or below any address chosen on a 4k boundary. Located between U-9 and U-19 is a jumper that determines whether to deselect at and above a given address or below that given address. If the center post is jumpered to the left post, then the memory board will be deselected at and above a given address. If this option is not used, remove any jumpers from this area.

The 4k boundary address is determined by the jumper area located between U-13 and U-14. The center columns of posts from bottom to top are A12-A15 respectively. The left column is Vcc, the right column is ground. To establish an address, jumper the corresponding address bits desired to ground. For example, to set the address desired to C000H, jumper A14 and A15 to ground and A12 and A13 to Vcc.

EXPANDING FROM 64K TO 256K

1. Remove U-35, an LM340T-12.0, and replace it with an LM340T-5.0. This supplies +5V to all RAM IC's.

2. Cut the trace between pin 3 of U-34 and the feed-thru pad immediately to the right. This issolates pin 9 of all the RAM IC's.

3. Below the RAM array there are two rows of 0.1uf decoupling capacitors. Remove the 16 capacitors in the bottom row (including the one at far right oriented vertically). This removes all decoupling from pin 9 of all RAM IC's. Also below the RAm array are four grops of two tantalum capacitors each. Remove the left capacitor in each group. This removes the decoupling from pin1 of all RAM IC's.

4. Install a 51 ohm resistor immediately to the right of U-30 so that there are now three resistors in that area. This connects A7 to pine 9 of all RAM IC's.

5. Below U-34 and to the left of U-33 are three feed-thru pads. Cut the trace that now connects the center pad to the right pad and install a jumper from the center pad to the left pad. This ties pin 1 on all RAM IC's to +5V.

6. If the RAM's used require 256 refresh cycles, locate the jumper pad between U-18 and U-25. Cut the trace between the center pad and the right pad, install a jumper from the center pad to the left pad. If the RAM's used require 128 refresh cycles, skip this step.

7. Between U-30 and U-15 are three jumper pads. Cut the trace between the center and left pads. Install a jumper between the center and right pads. This connects A14 to U-30.

8. Between U-6 and U-7 are six jumper pds. Cut the traces between the center two pads and the top two pads. Install jumpers from the center pads to the bottom two pads.

USING +5V ONLY 16K RAM'S

1. Perform steps 1, 2, and 5 of "Expanding from 64k to 256k".

2. Jumper the feed-thru pad mentioned in step 2 to ground. This grounds pin 9 of all RAM IC's.

BANK SELECT FOR 256K

The bank select scheme for the 256k memory board provides four 64k banks, all starting at 0000H. By jumpering U-31 appropriately, there are eight possible banks allowed in the system. Refer to the section on bank select for 64k for more information on the 16-pin header setup.

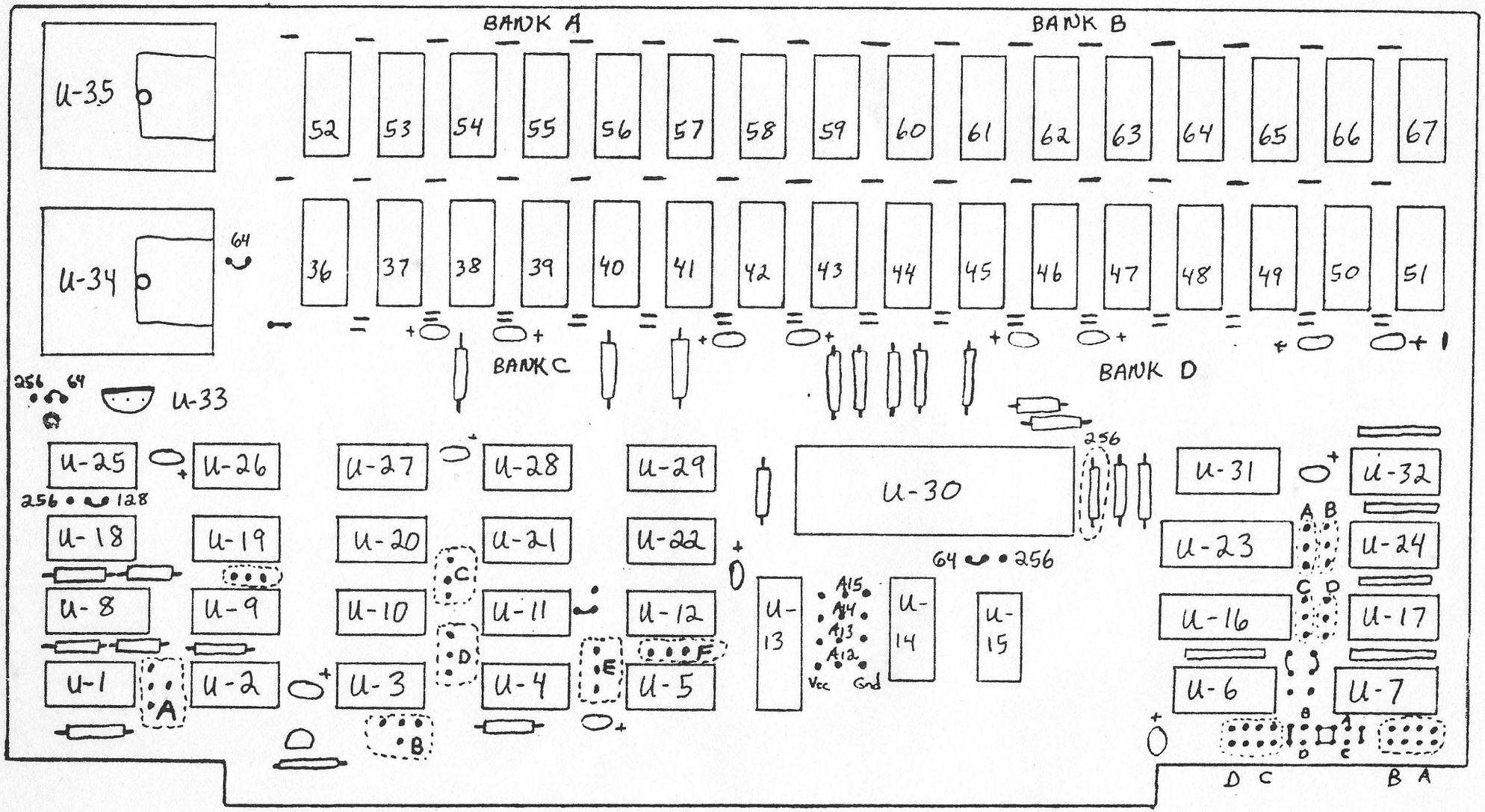
The four banks onboard can still be enabled or disabled on system RESET, as on the 64k version.

The jumpers for bank addressing on the 64k memory board are now used strictly as disable jumpers. If any one of the two possible address jumpers are installed for any given bank, that bank will be disabled. To enable all banks on the 256k version, remove all addressing jumpers.

Each bank will still respond to PHANTOM* as on the 64k version except that on the 256k memory board all 64k bytes of the chosen bank are disabled at once.

The 4k Block Deselect feature will also operate the same as on the 64k memory board. Additionally, it is possible on the 256k memory board to choose an address on any 4k boundary above which bank D will always be enabled, regardless of which bank is currently enabled. This simplifies some multi-user operating system implementations that require (for example) the top 16k in system memory be reserved for the operating system. To enable this option, remove any jumpers tht exist between posts in the jumper area between U-9 and U-19. Locate the three jumper pads between U-11 and U-12. Cut the trace between the center and left pads.

Install a jumper between the center and top pads.


BANK A
BANK B
BANK C
BANK D
U-35
U-34
U-33
52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67
36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51
64
256
64
256 128
U-25 U-26 U-27 U-28 U-29
U-18 U-19 U-20 U-21 U-22
U-8 U-9 U-10 U-11 U-12
U-1 U-2 U-3 U-4 U-5
U-30
256
64 256
U-31 U-32
U-23 U-24
U-16 U-17
U-6 U-7
U-13 U-14 U-15
A15 A14 A13 A12 Vcc Gnd
A B C D E F
D C B A