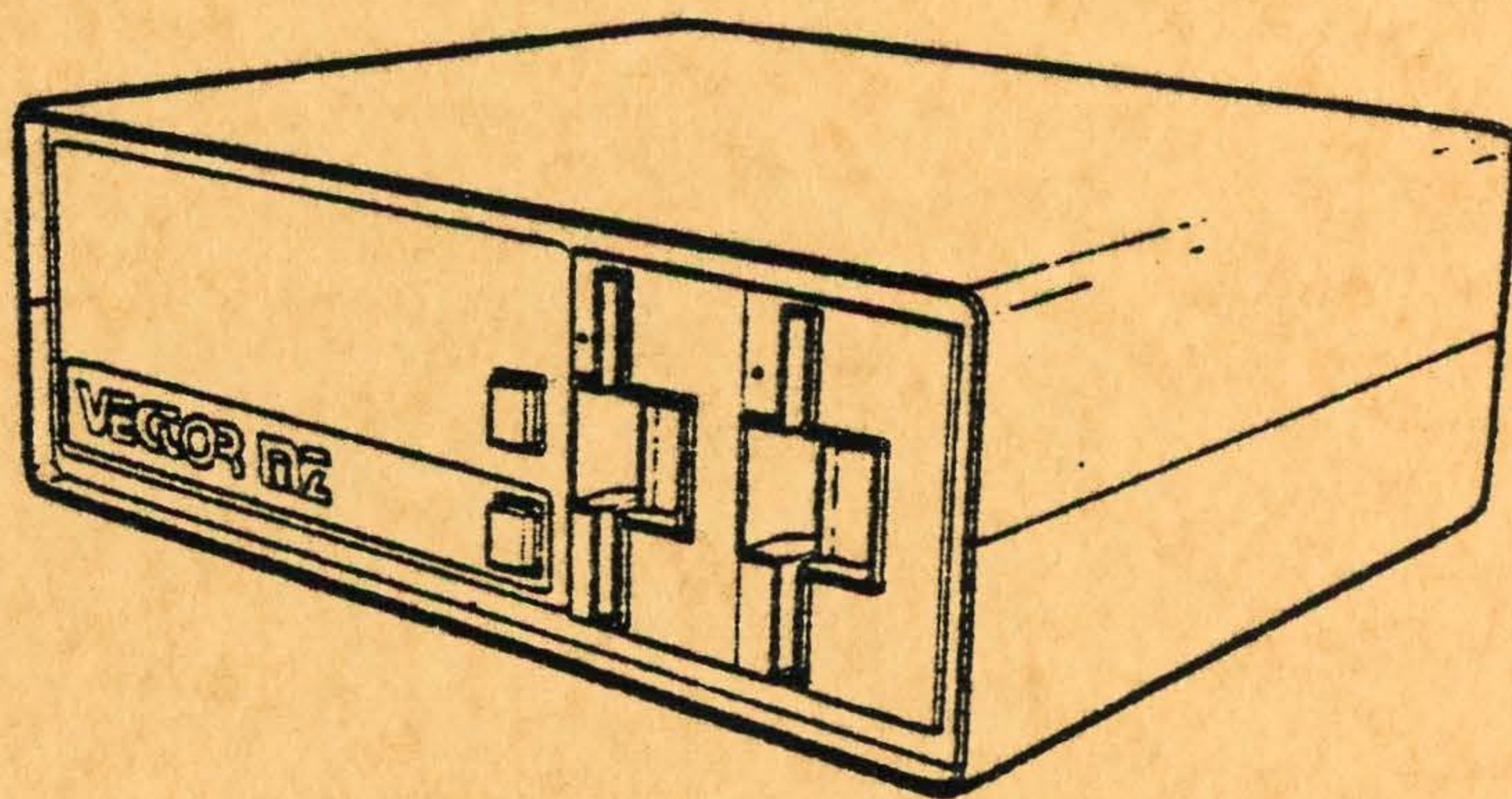
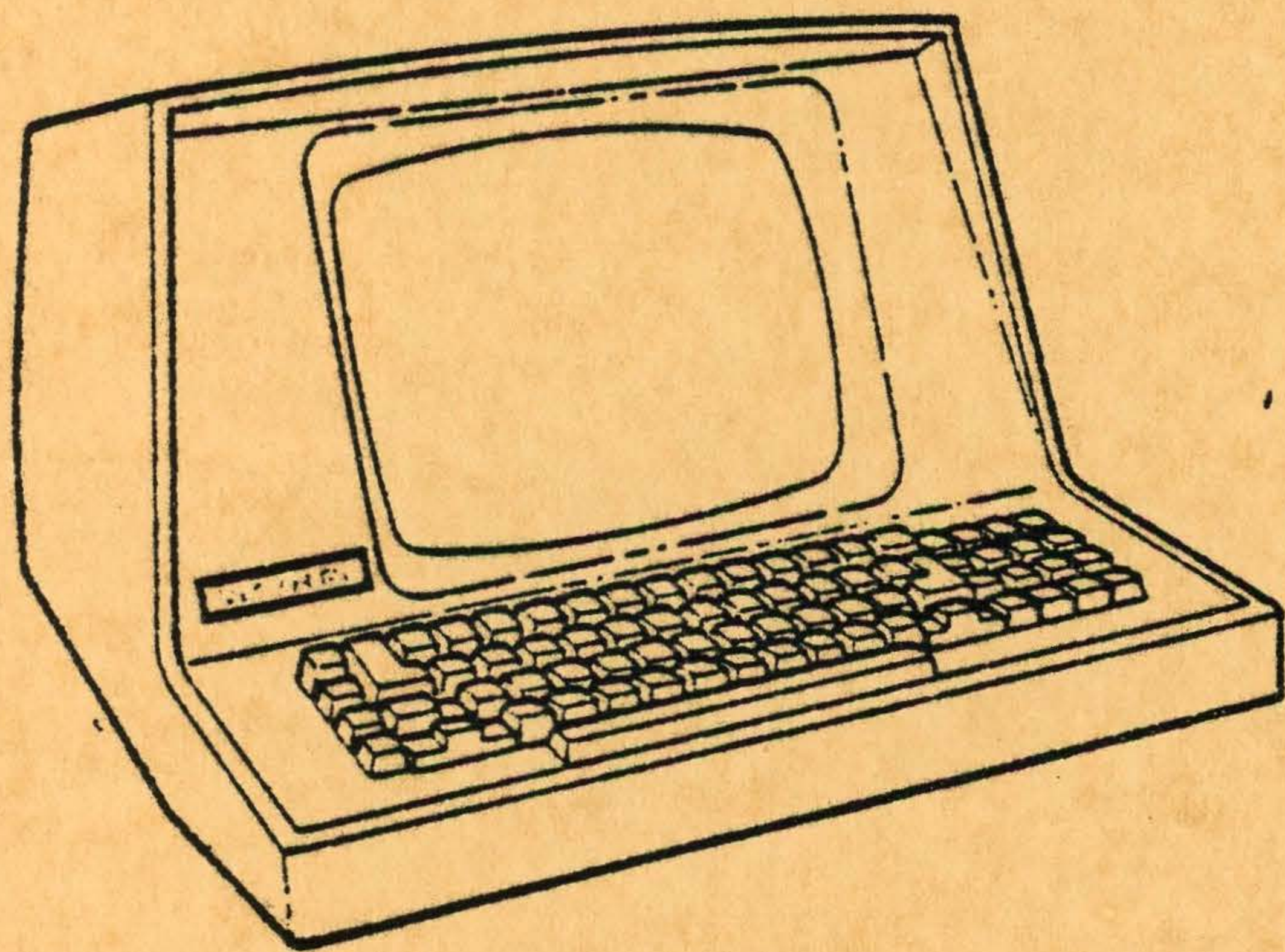


HIGH RESOLUTION GRAPHICS

USERS MANUAL



VECTOR
VECTOR GRAPHIC, INC.

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I. INTRODUCTION

1.1 SPECIFICATIONS

Bus Compatibility	S-100
Other Boards Required	Vector Graphic 8K Static RAM board Uses all 8K for screen memory
Monitor Required	Standard raster scan, taking composite video (cannot use Vector Graphic Mindless Terminal)
Resolution	Digital: 256 Horizontal 240 Vertical Gray Scale: 128 Horizontal 120 Vertical
Output	Composite video, conforming to RS-170
Switch Selectable Options	Digital or 16-level gray scale mode CPU wait state during screen refresh
Other Controls	Horizontal position
Other Features	Card extractors Cables for connection to 8K board
Power	8V @ 0.6A 8K Memory: 8V @ 1.5A additional

1.2 DESCRIPTION OF THE BOARD

The Vector Graphic High Resolution Graphics Display board provides the small computer user with the ability to generate graphic displays with 256 by 240 resolution elements in the digital mode or 128 by 120 pixels with 16 intensity levels in the gray scale mode. The 1:1 aspect ratio is compatible with the format for slow scan TV. The board is equally useful to display the output of a fast scan TV digitizer. Possible applications include image processing, feature extraction, storage scope replacement for inherently slow scans such as spectrum analyzers, transmission of images over voice

lines for remote surveillance, automated design, and a multitude of applications that the low cost of microcomputers and advanced peripherals will make practical for the first time.

This board must be used in conjunction with a Vector Graphic 8K Static RAM board, ordered separately. The TV monitor used with the board must be a standard TV monitor, which accepts COMBINED video and sync. The Vector Graphic Mindless Terminal cannot be used, although it may be included in the same system using a separate video board.

A variety of software is available for graphic displays, some of which is available from your dealer. Other software is available in the personal computing literature which has been written for older, lower resolution displays but which can be adapted with minor changes. At the back of this manual you will find a program which includes an x-y driver which plots or erases points on the screen which may be addressed as locations on a 256 by 256 grid. Such a driver is the basis for adapting most software.

If you develop programs for the display that would be of interest to others, please send us a source listing with an explanation on either tarbell tape, Micropolis disk, North star disk, or CP/M disk and we will try to include a limited amount under your authorship in future manuals.

1.3 DESCRIPTION OF THE MANUAL

This manual provides a discussion of the theory of operation of the High Resolution Graphics Display board, and a User's Guide explaining how to install and use the board.

II. THEORY OF OPERATION

The High Resolution Graphics Display board consists of the circuitry necessary to display high quality images and patterns on a standard raster scan TV monitor.

The Graphics board is used in conjunction with a Vector Graphic 8K Static Ram board (used for screen memory) and the two boards are interconnected by means of 5 jumper cables which are included with the Graphics board.

The High Resolution Graphics Display can be divided into five functional groups:

Horizontal sync

Vertical sync

Memory

Memory control

Video

2.1 HORIZONTAL SYNC

The horizontal sync circuitry consists of the necessary logic to produce a suitable horizontal synchronization signal for use by a TV monitor. A quartz crystal controlled oscillator produces a frequency of 14.318 MHz which must be counted down to produce the required horizontal sync pulse at the 15.75 KHz rate. The 14.318 MHz clock is first divided by two by A5 and the resulting 7.875 MHz is applied to the horizontal counters formed by A3 and A4. Using 74LS161 synchronous 4 bit binary counters which are preset to 56 results in a count of 456, thus the resultant output is 15.75 KHz. Preloading of the horizontal counters occurs when A4 generates a carry signal and A5-10 is set at the next clock occurrence. The resulting output is logically ANDed by B5 with the carry signal and applied to counters A3-9 and A4-9. As the 74LS161 requires that presetting be synchronous with the clock, this circuitry fulfills this requirement.

The same signal that is used to preset the counters is applied to A2, a 74221 dual one-shot, to produce a variable horizontal delay signal adjustable by the 10K potentiometer located at the top edge of the board. The 74221 timing components are adjustable to produce a delay of 2-20 micro-seconds. The trailing edge of the horizontal delay signal is used to fire the other half of the 74221 one-shot which is set up to produce a 5 micro-second horizontal sync pulse. This signal, with the horizontal delay signal, is then applied to gating logic formed by A1 to create a combined horizontal and vertical sync signal.

The horizontal blanking signal is formed by B3, a 74LS109 flip flop. The output from A5-10, count C7, is applied to the J and K inputs of B3. B3 is set by the leading edge of C1 and remains set for the duration of C7 which is 35.75 micro-seconds, at which time it is reset and blanking occurs for approximately 27 micro-seconds.

2.2 VERTICAL SYNC

The vertical sync circuitry on the High Resolution Graphics Display board consists of counting and timing logic to generate proper sync and blanking signals for use by a TV monitor.

Using the 15.75 KHz horizontal sync signal as a clock for the vertical counters formed by two 74LS161 synchronous 4 bit binary counters and flip flop B3, a total count of 262 is obtained. A proper vertical sync signal is created from counts 240 to 244 and vertical blanking occurs from counts 240 to 262. Counts 240-244 are created by the logical AND of C10, C11 and count 240. Count 240 is the carry output of counter B1. The leading edge of vertical sync causes the latch created by B4 to be set and generates vertical blank. This latch remains set until 261 occurs which clears the latch and also presets the vertical counters. 261 is created by the logical AND of C8, C10 and the carry outputs of counters B1 and B2.

The vertical sync signal is applied to the gating logic formed by A1 and the vertical blanking is applied to nand gate B5 and logically OR'ed with the horizontal blanking signal.

2.3 MEMORY CONTROL

The High Resolution Graphics Display board has the circuitry required to multiplex the address and data signals to the 8K memory board used as screen refresh memory. The board logic must be able to allow memory to be addressed by both the CPU and the video counters formed by the horizontal and vertical counters and allow transfer of data to and from the CPU as well as data to the TV monitor in the form of video information.

By replacing the control logic IC's on the 8K memory board with the Graphic board jumper cables the task of address and data control is transferred to the Graphics board.

The address lines to the memory are now multiplexed with the outputs of the video counters thus allowing access to the memory array by the CPU or the video counters. Board addressing is still determined by the address select switch on the 8K board as previous. If the user required access to the screen memory by the CPU, control would be gained when BOARD ENABLE was true, thus setting the tri state enables on the video counter buffers off and enabling the CPU bus address buffers.

The R/W control signal to the memory array is now formed by the logical AND of BOARD ENABLE and MWRITE. When data is to be read into the CPU, the data bus drivers are enabled by the AND of BOARD ENABLE, SMEMR and PDBIN.

2.4 VIDEO

The high resolution graphics board is capable of generating displays in two general formats:

Digital (on/off) mode

Gray scale mode

In the digital mode the display screen is defined as 256 horizontal x 256 vertical screen positions. Each element is equal to one bit of memory.

256 (horizontal) x 256 (vertical) = 65,536 bits
= 8192 bytes.

Since it is impractical to display the entire vertical field, only 240 vertical positions are actually displayed.

The memory data to be converted to a video compatible format is read byte by byte in a sequential manner as accessed by the addresses established by the video counters.

This data is received on the graphics board by an eight bit parallel shift register formed by D4 and D5. Data is clocked into this register by the trailing edge of count C0 which occurs about 558 nsec after the address is true. This permits enough time for memory access requirements to be fulfilled. The latched data is then applied to a multiplexer, D6, which creates two 4 bit nibbles and outputs the most significant nibble first, least significant nibble last, to a 4 line to 1 line multiplexer which selects and outputs a serial stream of data at a 3.58 MHz rate.

In the gray scale mode of operation the 4 bit nibbles of data drive a 4 bit digital-to-analog convertor formed by a 7406 and appropriate scaling resistors to generate 16 levels of gray scale including black and white. The current from these resistors is applied to a current mirror consisting of Q1 and Q2 which produces a current in the collector of Q2 identical to the current in the collector/base of Q1. Since the input impedance is very low, the input currents are linearly independent of one another. The output current produces a video output and with the other sections of the 7406, a composite video signal including sync and blanking is formed.

VIDEO

III. USERS GUIDE

3.1 INSTALLATION

The High Resolution Graphics Display board is used in conjunction with a Vector Graphic 8K static RAM board. The 8K board must be ordered as a separate item, so that user's already possessing one can use the one they have.

To connect the two boards together first remove the IC's installed in locations J3, J4, J5, J6, and J7 on the 8K memory board.

On a flat surface place the 8K memory component-side up. Gently place the Graphics board on top of the memory board so that the dip connectors line up with the empty sockets on the memory board. Carefully insert the dip connector from J7 on the Graphics board into the socket marked J7 on the memory. In a similar manner repeat for J3 to J6. The results should look exactly as shown in Figure 1.

The two boards may now be inserted in your motherboard.

High Resolution Graphics Board Users Manual

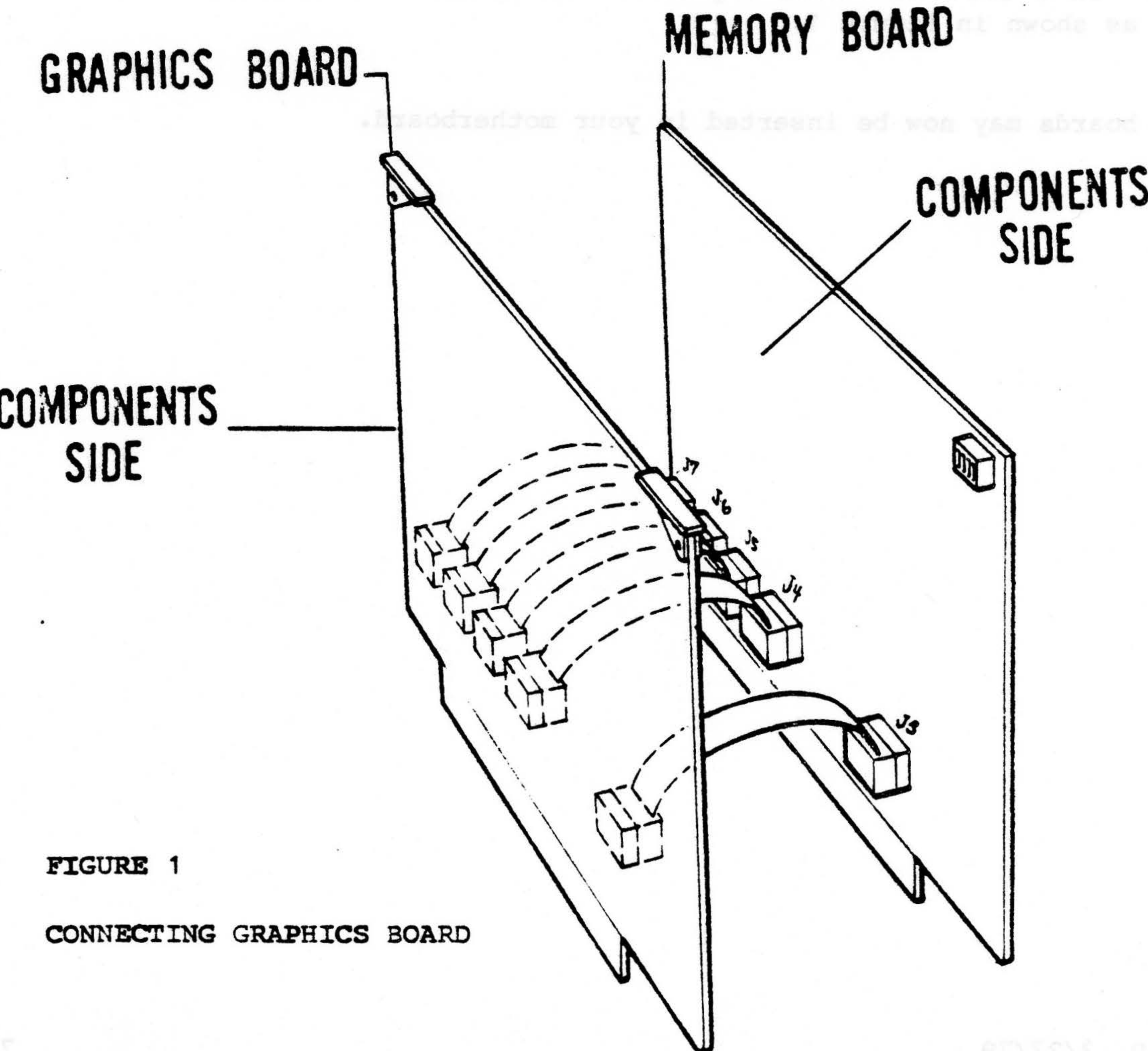
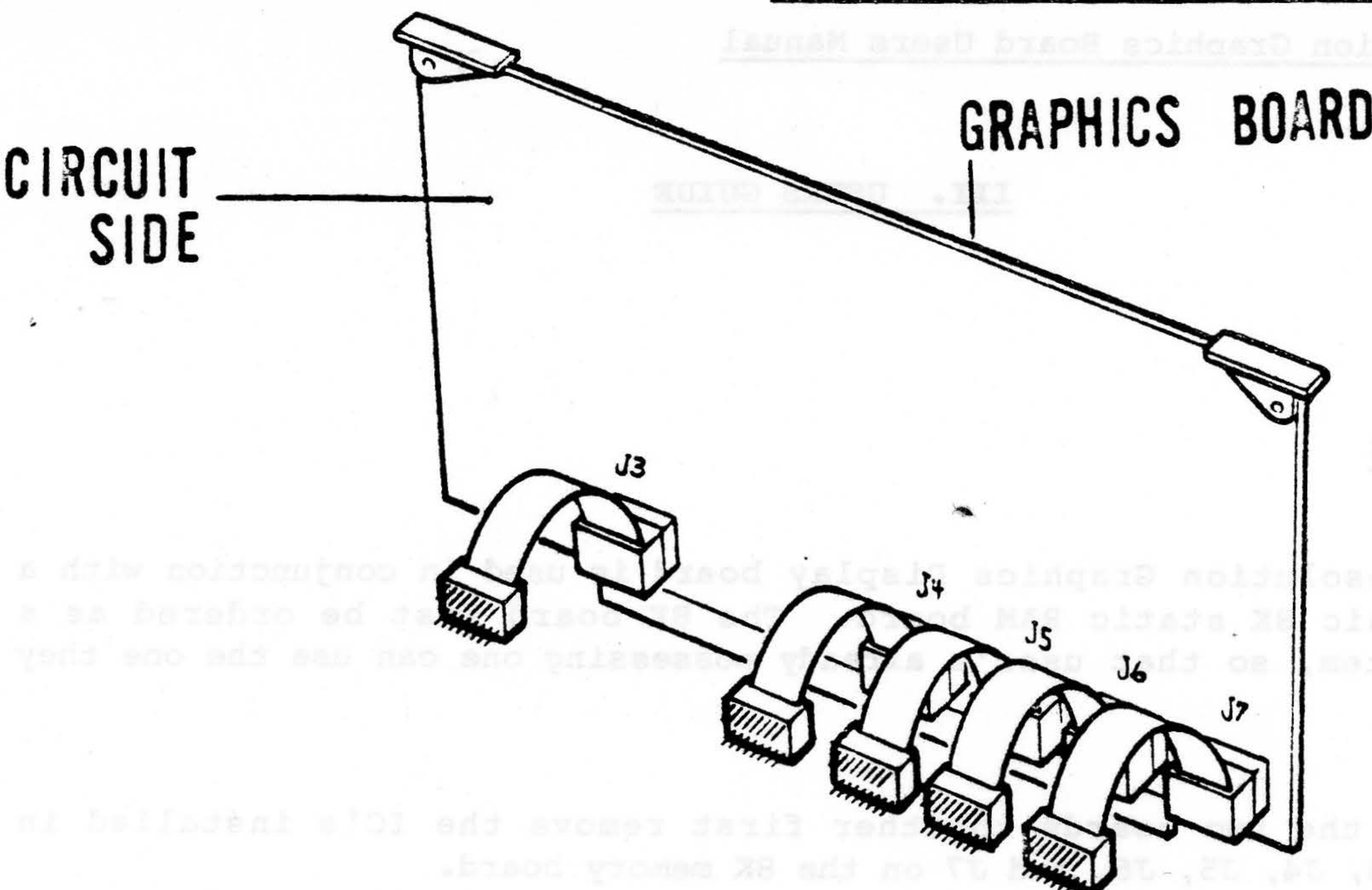


FIGURE 1
CONNECTING GRAPHICS BOARD

3.2 MEMORY ADDRESS

On the upper right-hand corner of the 8K board, you will find a dipswitch that controls the memory address space occupied by the 8K board. You may use any 8K segment up to FFFFH available in your system. In 32K systems, A000 to BFFF is usually used, while in the more recent 48K systems, E000 to FFFF must be used. The dipswitch is set as shown in the following table. Press a lever up for 1, down for 0. The most significant digit (A15) is on the left edge of the switch, and the digits continue to the right in the same order as in the table. The right-hand lever is not used for addressing -- it MUST be pressed up. (The down position write-protects the board, obviously not desired for this application.) Refer to the manual for the 8K board for information about other features of that board.

<u>ADDRESS RANGE</u>	<u>SWITCH SETTING (1=ON)</u>
0000 - 1FFF	0001
2000 - 3FFF	0011
4000 - 5FFF	0101
6000 - 7FFF	0111
8000 - 9FFF	1001
A000 - BFFF	1011
C000 - DFFF	1101
E000 - FFFF	1111

MEMORY ADDRESS SELECT ON 8K BOARD

3.3 DIGITAL OR GRAY SCALE

The dip switch on the High Resolution Graphics Display board permits the user to choose between digital video output (256 horizontal x 240 vertical) or gray scale video (128 horizontal x 120 vertical). Refer to Figure 2, below. Of the two levers identified as Digital Video and Gray Scale, one must be in the up (ON) position, and the other must be in the down (OFF) position. (If they are both in the ON position, the board will not work properly, but nothing will be harmed.)

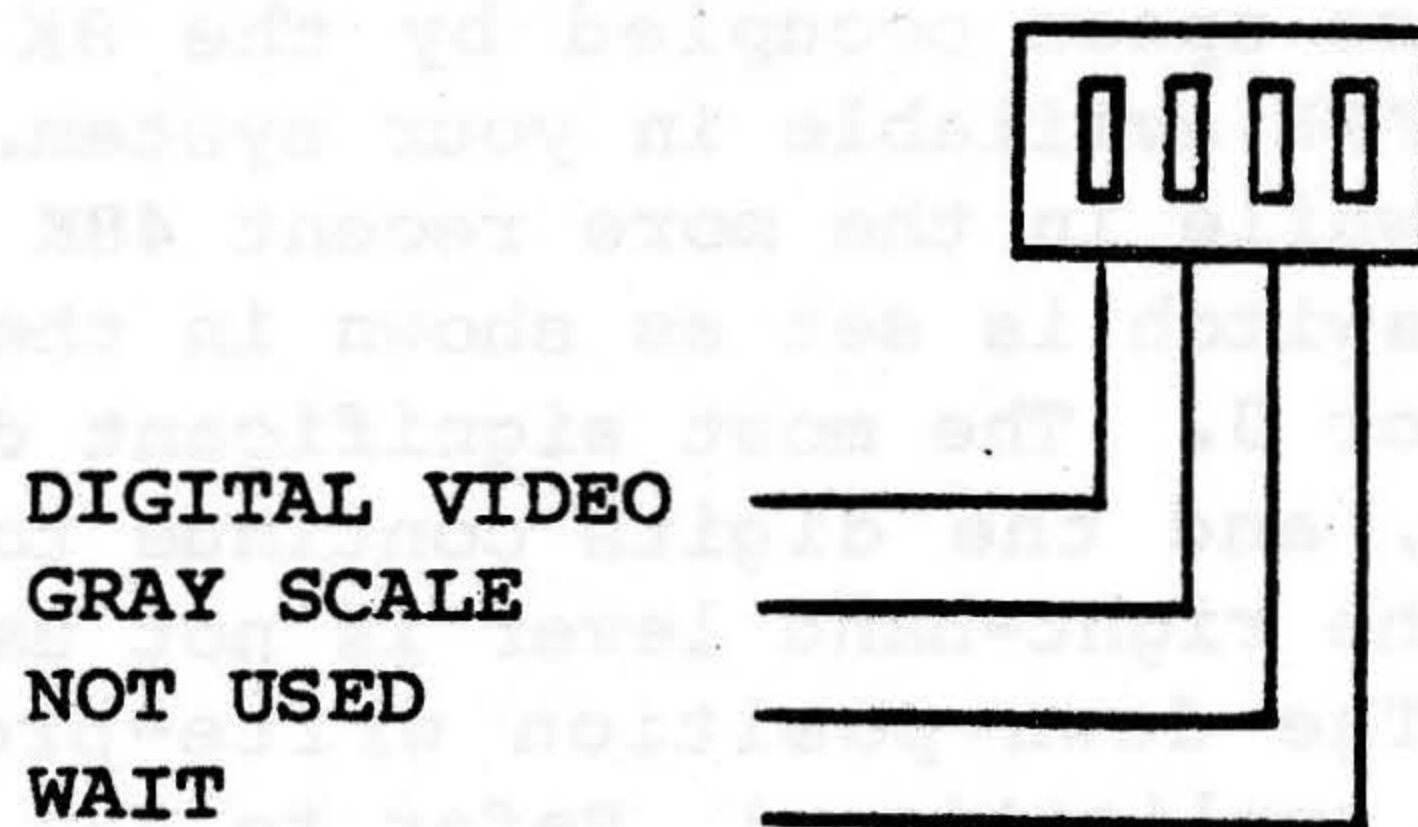


FIGURE 2 DIPSWITCH ON GRAPHICS BOARD

3.4 WAIT STATE

As shown in Figure 2, the dipswitch on the Graphics board also allows the user to choose between normal operation with no wait states or select a wait signal output. If the wait state is selected, it permits glitch free updating of the display by only allowing memory to be accessed during horizontal blanking. If the memory is accessed during the unblanked portion of the horizontal sweep, the CPU enters a wait state. When blanking occurs, the CPU is permitted to access memory. Note that if the wait signal is generated, consideration must be given to devices such as disk drives which may not be able to operate with wait states. Thus if graphics data is to be stored or retrieved from disk, it should be first loaded into normal RAM and then moved into the graphics memory. Of course if the wait is not selected, memory operates at full speed.

3.5 VIDEO OUTPUT

The output video is available on the two pin connector J1 located at the top of the Graphics board. Ground is the right hand pin when you are facing the component side of the board.

3.6 PROGRAMMING DISPLAY MEMORY

The correspondence between the contents of the 8K memory segment and the image on the screen is as follows. (A "pixel" is an area on the screen consisting of a 2 X 2 square of digital points or an equally sized area of gray coloration.)

In the gray scale mode, the second 4 bits in memory produce a gray scale pixel in the upper left-hand corner of the screen. The first 4 bits produce the pixel immediately to the right of this, as shown in Figure 3 below. Moving to the right, this pattern is repeated for the next higher byte in memory. The first line of 128 pixels on the screen are thus produced by the first 64 bytes of memory; the second 64 bytes then produce the second line on the screen, and so on. This continues for 120 lines of pixels, which use up most of the 8K. The remaining part of the 8K is NOT displayed. (I.e. the last 200 Hex bytes of the memory space are not used.)

In the digital mode, the second 4 bits in memory are mapped into the first pixel in the upper left-hand corner of the screen as shown below in Figure 3. The first 4 bits are mapped into the second pixel, also as shown in Figure 3. This continues from left to right and down the screen, just as in gray scale mode. The important point to remember is that the points are stored in memory pixel by pixel. As with the gray scale mode, the last 200 Hex bytes of the 8K memory space are not displayed. At the end of this manual, you will find a demonstration program. Near the end of this program you will find an XY plotter which can be used to set or erase any point (in digital mode) using X-Y coordinates.

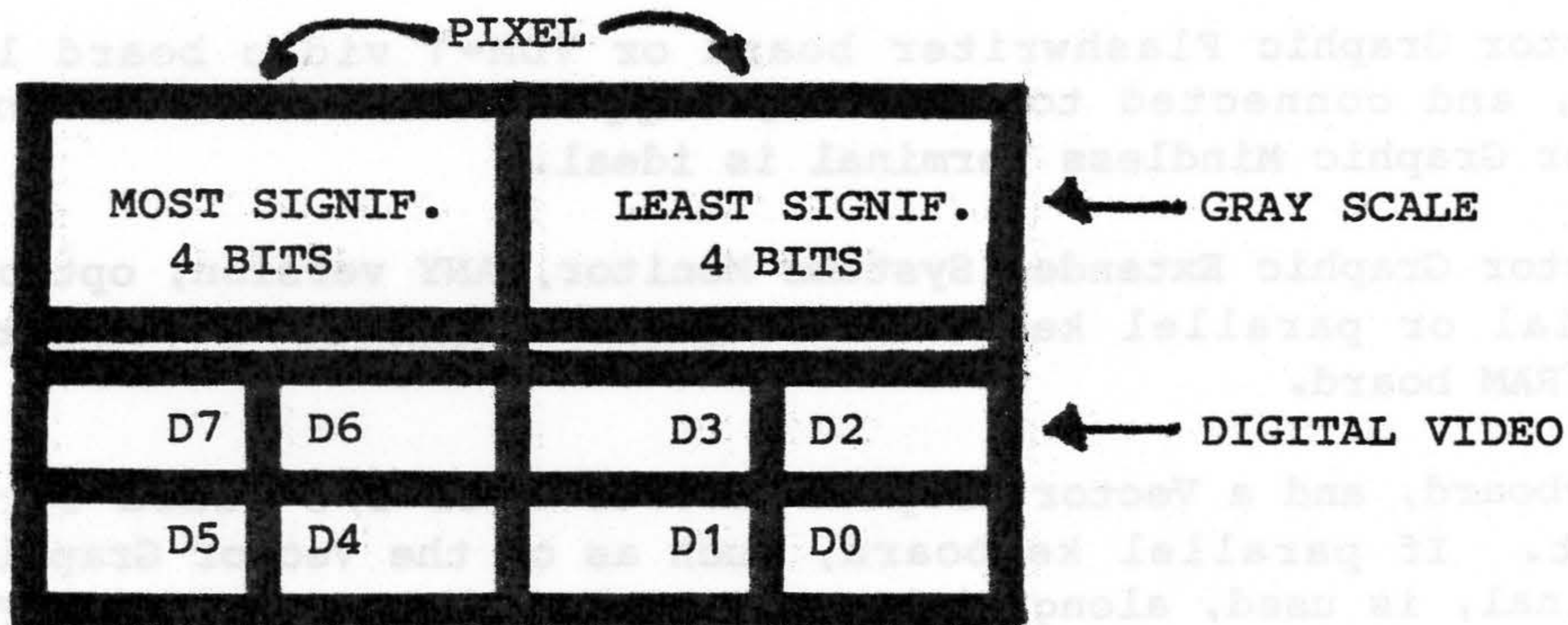


FIGURE 3 MAPPING OF MEMORY BY GRAPHICS BOARD

3.7 GRAPHICS DEMO DISK

As a separate item, a Graphics Demo Disk can be purchased that shows off the versatility of the High Resolution Graphics Display board. It includes a number of high resolution images, in both digital and gray scale modes, produced by TV digitizers, an alphanumeric output driver enabling use of the board as a terminal, and several demonstration programs. Among these programs is a simple language called "ROBOT" which can be used to create remarkable patterns on the screen.

3.8 ROBOT

The program entitled ROBOT is presented in the following pages as an Assembler listing. The code is also available on the Graphics Demo Disk, purchased separately. The use of this program is explained fully in the September, 1977 issue of Dr. Dobbs Journal. However, once the code is loaded and running, simply depress E on the keyboard in order to view a demonstration of its capabilities. If you then wish to go further, the program allows you to create infinite varieties of patterns such as the ones E will cause displayed.

The minimum equipment required is:

S-100 computer such as Vector MZ, or Vector 1, 1+, or 1++.

At least 8K of memory beginning at 0000.

A Vector Graphic Flashwriter board or VDM-1 video board located at D000, and connected to a memory mapped monitor. Flashwriter plus Vector Graphic Mindless Terminal is ideal.

A Vector Graphic Extended Systems Monitor, ANY version, option CV or EV (serial or parallel keyboard respectively), on a Vector Graphic PROM/RAM board.

A keyboard, and a Vector Graphic Bitstreamer I/O board for keyboard input. If parallel keyboard, such as on the Vector Graphic Mindless Terminal, is used, along with a Flashwriter board, then the Flashwriter keyboard port can be used instead of a Bitstreamer board.

High Resolution Graphics Display board with 8K of memory addressed at A000 or E000.

A second video monitor, one accepting combined video and sync, connected to the Graphics board.

Load the code at 0000 by any means possible. (Using the Demo Disk, just type "ROBOT" while under MDOS.) If the Graphics board is addressed at E000, then the program must be patched at two places before it can be used. Change 0296H and 0362H from A0 to E0.

Once the program is running, you can create your own displays by creating "macros". If you type control-X, then the program will save these macros within itself so that they become permanent. Remember to save the new program on disk or tape so that they are not lost.

3.9 A CHARACTER GENERATOR AND DISPLAY PROGRAM

Following ROBOT in this manual, you will find the listing for a character generator and display program. This program is used to display ASCII characters on the screen via the High Resolution Graphics Display board. As with ROBOT, it must be patched to run at E000 if the Graphics board is addressed at E000. The appropriate steps have the constants "BLOCK" and "BLOC" in them, which must be changed from A000 and A0 to E000 and E0 respectively. To make it easy, reassemble the program, changing only the EQUATES at the beginning. To use the program, call it with the desired ASCII code in the A register.

This program DOES NOT emulate standard memory mapped video boards. The High Resolution Graphics Display Board cannot display more than 32 5 X 7 characters on one line of the screen.

```

0000 0010 * INTERACTIVE ROBOT CONTROL LANGUAGE *
0000 0020 * WITH VECTOR GRAPHIC HI RES PLOT ROUTINE *
0000 0030 * DR. DOBBS, SEPT. 1977.
0000 0040 * R.S.HARP 1/29/78
0000 0050 *
0000 0060 * DEFINITIONS AND CONSTANTS
0000 0070 *
0000 0090 FLASH EQU OD000H FLASHWRITER
0000 0100 FLSH EQU ODOH
0000 0110 HIRES EQU OA000H
0000 0120 HRES EQU OAOH
0000 0140 STACK EQU 1FF0H STACK LOCATION
0000 0150 SEED EQU STACK
0000 0155 BORW EQU SEED+2
0000 0158 X EQU SEED+3
0000 0160 Y EQU SEED+4
0000 0162 DX EQU SEED+5
0000 0164 DY EQU SEED+6
0000 0165 SFLAG EQU SEED+7
0000 0166 PTCN EQU OC098H MONITOR OUTPUT
0000 0170 CNTLC EQU OC0DCH MONITOR CNTL C
0000 0180 *
0000 0190 * COMMANDS AND OPERATORS *
0000 0200 *
0000 0210 * A ACCUMULATOR
0000 0220 * B BLACK TRACE
0000 0230 * C CLEAR SCREEN
0000 0240 * D DEFINE MACRO
0000 0250 * F FORWARD ONE STEP
0000 0260 * H HOME TO CENTER
0000 0270 * N FACE NORTH
0000 0280 * R ROTATE 45 DEG RIGHT
0000 0285 * S SENSE TRACE
0000 0290 * T TEST ACC FOR ZERO
0000 0300 * W WHITE TRACE
0000 0310 * ' ' NO OPERATION
0000 0320 * (,) AS IN ALGEBRA
0000 0330 * DEL BACKSPACE
0000 0340 * ? RANDOM CHOICE
0000 0350 * +,- ACC OPERATIONS
0000 0360 * (X) SAVE PROG & RETURN TO MON
0000 0370 *
0000 0380 *
0000 31 F2 1F 0390 START LXI SP,SEED+2
0003 CD B0 02 0400 CALL WHITE+1
0006 CD C0 02 0410 CALL NORTH+1
0009 AF 0415 XRA A
000A D3 C8 0420 OUT OC8H
000C CD 92 02 0422 CALL CLEAR+1
000F CD B7 02 0424 CALL HOME+1
0012 11 00 04 0430 LXI D,MENU
0015 21 00 D0 0440 LXI H,FLASH
0018 1A 0450 I1 LDAX D
0019 77 0460 MOV M,A

```

```

001A 13
001B 23
001C 7C
001D FE D4
001F C2 18 00
0022 21 41 3D
0025 22 3A D0
0028 21 30 30
002B 22 3C D0
002E 22 3E D0
0031 31 F0 1F
0034 21 00 D0
0037 06 20
0039 36 20
003B 23
003C 05
003D C2 39 00
0040 0E 7F
0042 CD B9 00
0045 CA 37 00
0048 60
0049 68
004A 11 00 D0
004D CD 5D 00
0050 21 00 D0
0053 50
0054 58
0055 06 FF
0057 CD 5D 00
005A C3 34 00
005D
005D CD 8D 00
0060 CD DC C0
0063 C2 31 00
0066 E5
0067 CD D1 00
006A 78
006B C2 71 00
006E B7
006F E3
0070 C9
0071
0071 B7
0072 E1
0073 C8
0074 E5
0075 CD B9 00
0078 C2 8B 00
007B E5
007C 21 C0 F7
007F 39
0080 7C
0081 B7
0082 FA 31 00
0085 E1
0086 23

```

```

0470 INX D
0480 INX H
0490 MOV A,H
0500 CPI FLSH+4
0510 JNZ I1
0520 LXI H,'=A'
0530 SHLD FLASH+3AH
0540 LXI H,'00'
0550 SHLD FLASH+3CH
0560 SHLD FLASH+3EH
0570 DIRCT LXI SP,STACK
0580 D1 LXI H,FLASH
0590 D2 MVI B,32
0600 D3 MVI M,' '
0610 INX H
0620 DCR B
0630 JNZ D3
0640 MVI C,7FH
0650 CALL FIND
0660 JZ D2
0670 MOV H,B
0680 MOV L,B
0690 LXI D,FLASH
0700 CALL RCMD
0710 LXI H,FLASH
0720 MOV D,B
0730 MOV E,B
0740 MVI B,-1
0750 CALL RCMD
0760 JMP D1
0770 *
0780 RCMD CALL GETCH
0790 CMD CALL CNTLC
0800 JNZ DIRCT
0810 PUSH H
0820 CALL RESRV
0830 MOV A,B
0840 JNZ C1
0850 ORA A
0860 XTHL
0870 RET
0880 *
0890 C1 ORA A
0900 POP H
0910 RZ
0920 PUSH H
0930 CALL FIND
0940 JNZ C2
0950 PUSH H
0960 LXI H,-DANGR
0970 DAD SP
0980 MOV A,H
0990 ORA A
1000 JM DIRCT
1010 POP H
1020 INX H

```


0087	23	1030	INX	H	00DD	23	1590	INX	H		
0088	CD 5D 00	1040	CALL	RCMD	00DE	23	1600	INX	H		
008B	E1	1050	POP	H	00DF	05	1610	DCR	B		
008C	C9	1060	RET		00E0	C2 D8 00	1620	JNZ	V1		
008D		1070	*		00E3	C1	1630	POP	B		
008D	7B	1080	GETCH	MOV	A,E	00E4	21 22 02	1640	LXI	H,CMD09	
008E	E6 1F	1090		ANI	31	00E7	3E 39	1650	DIGIT	MVI	A,'9'
0090	FE 1F	1100		CPI	31	00E9	B9	1660		CMP	C
0092	D2 31 00	1110		JNC	DIRCT	00EA	D8	1670		RC	
0095	B2	1120		ORA	D	00EB	79	1680		MOV	A,C
0096	CA 9C 00	1130		JZ	G1	00EC	D6 30	1690		SUI	'0'
0099	3E 7F	1140		MVI	A,7FH	00EE	D8	1700		RC	
009B	12	1150		STAX	D	00EF	BF	1710		CMP	A
009C	7C	1160	G1	MOV	A,H	00F0	C9	1720		RET	
009D	B5	1170		ORA	L	00F1		1730	*		
009E	C2 B0 00	1180		JNZ	G3	00F1	7E	1740	V2	MOV	A,M
00A1	CD 51 01	1190	G2	CALL	RNDB	00F2	23	1750		INX	H
00A4	CD DC C0	1200		CALL	CNTLC	00F3	66	1760		MOV	H,M
00A7	CA A1 00	1210		JZ	G2	00F4	6F	1770		MOV	L,A
00AA	E6 7F	1220		ANI	7FH	00F5	C1	1780		POP	B
00AC	4F	1230		MOV	C,A	00F6	C9	1790		RET	
00AD	C3 B2 00	1240		JMP	G4	00F7		1800	*		
00B0		1250	*			00F7	C9	1810	CMDBL	RET	
00B0	4E	1260	G3	MOV	C,M	00F8		1820	*		
00B1	23	1270		INX	H	00F8	CD 8D 00	1830	CMDD	CALL	GETCH
00B2	7A	1280	G4	MOV	A,D	00FB	E5	1840		PUSH	H
00B3	B3	1290		ORA	E	00FC	CD D1 00	1850		CALL	RESRV
00B4	C8	1300		RZ		00FF	CA 31 00	1860		JZ	DIRCT
00B5	79	1310		MOV	A,C	0102	78	1870		MOV	A,B
00B6	12	1320		STAX	D	0103	B7	1880		ORA	A
00B7	13	1330		INX	D	0104	C2 0B 01	1890		JNZ	CD1
00B8	C9	1340		RET		0107	E1	1900		POP	H
00B9		1350	*			0108	C3 5D 00	1910		JMP	RCMD
00B9	D5	1360	FIND	PUSH	D	010B		1920	*		
00BA	C5	1370		PUSH	B	010B	CD B9 00	1930	CD1	CALL	FIND
00BB	21 40 D0	1380		LXI	H,FLASH+40H	010E	C2 13 01	1940		JNZ	CD2
00BE	11 20 00	1390		LXI	D,32	0111	36 7F	1950		MVI	M,7FH
00C1	06 1E	1400		MVI	B,30	0113	C5	1960	CD2	PUSH	B
00C3	79	1410		MOV	A,C	0114	0E 20	1970		MVI	C,' '
00C4	BE	1420	F1	CMP	M	0116	CD B9 00	1980		CALL	FIND
00C5	CA CE 00	1430		JZ	F2	0119	C2 31 00	1990		JNZ	DIRCT
00C8	19	1440		DAD	D	011C	C1	2000		POP	B
00C9	05	1450		DCR	B	011D	71	2010		MOV	M,C
00CA	C2 C4 00	1460		JNZ	F1	011E	23	2020		INX	H
00CD	04	1470		INR	B	011F	36 3D	2030		MVI	M,'='
00CE	C1	1480	F2	POP	B	0121	23	2040		INX	H
00CF	D1	1490		POP	D	0122	EB	2050		XCHG	
00D0	C9	1500		RET		0123	E3	2060		XTHL	
00D1		1510	*			0124	06 00	2070		MVI	B,0
00D1	C5	1520	RESRV	PUSH	B	0126	CD 8D 00	2080		CALL	GETCH
00D2	06 13	1530		MVI	B,19	0129	3E 20	2090		MVI	A,' '
00D4	21 49 02	1540		LXI	H,TABL	012B	B9	2100		CMP	C
00D7	79	1550		MOV	A,C	012C	C2 34 01	2110		JNZ	CD3
00D8	BE	1560	V1	CMP	M	012F	1B	2120		DCX	D
00D9	23	1570		INX	H	0130	1B	2130		DCX	D
00DA	CA F1 00	1580		JZ	V2	0131	12	2140		STAX	D

NO. OF COMMANDS

0132 1B
 0133 12
 0134 CD 60 00
 0137 D1
 0138 06 FF
 013A C9
 013B
 013B CD 8D 00
 013E 79
 013F FE 29
 0141 C8
 0142 CD 60 00
 0145 C3 3B 01
 0148
 0148 CA 67 01
 014B CD 51 01
 014E C3 7B 01
 0151
 0151 E5
 0152 2A F0 1F
 0155 29
 0156 7D
 0157 D2 5D 01
 015A EE 2D
 015C 6F
 015D 22 F0 1F
 0160 E1
 0161 E6 01
 0163 C9
 0164
 0164 C2 6D 01
 0167 CD 5D 00
 016A C3 5D 00
 016D
 016D E5
 016E 2A 3C D0
 0171 7C
 0172 B5
 0173 2A 3E D0
 0176 B4
 0177 B5
 0178 E1
 0179 FE 30
 017B CA 89 01
 017E CD 5D 00
 0181 06 00
 0183 CD 5D 00
 0186 06 FF
 0188 C9
 0189
 0189 06 00
 018B CD 5D 00
 018E 06 FF
 0190 C3 5D 00
 0193
 0193 C8

2150 DCX D
 2160 STAX D
 2170 CD3 CALL CMD
 2180 POP D
 2190 MVI B,-1
 2200 RET
 2210 *
 2220 CMDLDP CALL GETCH
 2230 MOV A,C
 2240 CPI ')'
 2250 RZ
 2260 CALL CMD
 2270 JMP CMDLDP
 2280 *
 2290 CMDQM JZ SKIP
 2300 CALL RNDB
 2310 JMP TEST
 2320 *
 2330 RNDB PUSH H
 2340 LHLD SEED
 2350 DAD H
 2360 MOV A,L
 2370 JNC CQ1
 2380 XRI 2DH
 2390 MOV L,A
 2400 CQ1 SHLD SEED
 2410 POP H
 2420 ANI 1
 2430 RET
 2440 *
 2450 CMDT JNZ CT1
 2460 SKIP CALL RCMD
 2470 JMP RCMD
 2480 *
 2490 CT1 PUSH H
 2500 LHLD FLASH+3CH
 2510 MOV A,H
 2520 ORA L
 2530 LHLD FLASH+3EH
 2540 ORA H
 2550 ORA L
 2560 POP H
 2570 CPI '0'
 2580 TEST JZ T1
 2590 CALL RCMD
 2600 MVI B,0
 2610 CALL RCMD
 2620 MVI B,-1
 2630 RET
 2640 *
 2650 T1 MVI B,0
 2660 CALL RCMD
 2670 MVI B,-1
 2680 JMP RCMD
 2690 *
 2700 CMDPS RZ

0194 E5
 0195 CD F0 01
 0198 E1
 0199 3E 27
 019B BC
 019C C2 A7 01
 019F 3E 0F
 01A1 BD
 01A2 C2 A7 01
 01A5 E1
 01A6 C9
 01A7
 01A7 23
 01A8 0E 08
 01AA 29
 01AB 7C
 01AC D6 64
 01AE DA B3 01
 01B1 67
 01B2 23
 01B3 0D
 01B4 C2 AA 01
 01B7 4C
 01B8 7D
 01B9 21 3C D0
 01BC CD C6 01
 01BF 23
 01C0 79
 01C1 CD C6 01
 01C4 E1
 01C5 C9
 01C6
 01C6 36 2F
 01C8 34
 01C9 D6 0A
 01CB D2 C8 01
 01CE C6 3A
 01D0 23
 01D1 77
 01D2 C9
 01D3
 01D3 C8
 01D4 E5
 01D5 CD F0 01
 01D8 E1
 01D9 7C
 01DA B5
 01DB 2B
 01DC C2 A8 01
 01DF E1
 01E0 C9
 01E1
 01E1 CA 5D 00
 01E4 E5
 01E5 CD F0 01
 01E8 E1

2710 PUSH H
 2720 CALL GETA
 2730 POP H
 2740 MVI A,27H
 2750 CMP H
 2760 JNZ CPS1
 2770 MVI A,15
 2780 CMP L
 2790 JNZ CPS1
 2800 POP H
 2810 RET
 2820 *
 2830 CPS1 INX H
 2840 PUTA MVI C,8
 2850 P1 DAD H
 2860 MOV A,H
 2870 SUI 100
 2880 JC P2
 2890 MOV H,A
 2900 INX H
 2910 P2 DCR C
 2920 JNZ P1
 2930 MOV C,H
 2940 MOV A,L
 2950 LXI H,FLASH+3CH
 2960 CALL TWOD
 2970 INX H
 2980 MOV A,C
 2990 CALL TWOD
 3000 POP H
 3010 RET
 3020 *
 3030 TWOD MVI M,'0'-1
 3040 P3 INR M
 3050 SUI 10
 3060 JNC P3
 3070 ADI '0'+10
 3080 INX H
 3090 MOV M,A
 3100 RET
 3110 *
 3120 CMDMS RZ
 3130 PUSH H
 3140 CALL GETA
 3150 POP H
 3160 MOV A,H
 3170 ORA L
 3180 DCX H
 3190 JNZ PUTA
 3200 POP H
 3210 RET
 3220 *
 3230 CMDA JZ RCMD
 3240 PUSH H
 3250 CALL GETA
 3260 POP H

01E9	E3	3270	XTHL	023E	E3	3830	IT1	XTHL	
01EA	CD 8D 00	3280	CALL	023F	E5	3840		PUSH	H
01ED	C3 2E 02	3290	JMP	0240	C5	3850		PUSH	B
01F0		3300	*	0241	CD 60 00	3860		CALL	CMD
01F0	21 3C D0	3310	GETA	0244	C1	3870		POP	B
01F3	CD 8D 00	3320		0245	E1	3880		POP	H
01F6	E5	3330	NUMB	0246	C3 2E 02	3890		JMP	ITER
01F7	21 00 00	3340		0249		3900	*		
01FA	D5	3350	N1	0249	20	3910	TABL	DB	' '
01FB	3E 18	3360		024A	F7 00	3920		DW	CMDBL
01FD	BC	3370		024C	44	3930		DB	'D'
01FE	D2 02 02	3380		024D	F8 00	3940		DW	CMDD
0201	67	3390		024F	28	3950		DB	'('
0202	54	3400	N2	0250	3B 01	3960		DW	CMDLP
0203	5D	3410		0252	29	3970		DB	')'
0204	29	3420		0253	31 00	3980		DW	DIRCT
0205	29	3430		0255	7F	3990		DB	7FH
0206	19	3440		0256	31 00	4000		DW	DIRCT
0207	29	3450		0258	3F	4010		DB	'?'
0208	16 00	3460		0259	48 01	4020		DW	CMDQM
020A	79	3470		025B	54	4030		DB	'T'
020B	D6 30	3480		025C	64 01	4040		DW	CMDT
020D	5F	3490		025E	2B	4050		DB	'+'
020E	19	3500		025F	93 01	4060		DW	CMDPS
020F	D1	3510		0261	2D	4070		DB	'-'
0210	E3	3520	XTHL	0262	D3 01	4080		DW	CMDMS
0211	CD 8D 00	3530	CALL	0264	41	4090		DB	'A'
0214	CD E7 00	3540	CALL	0265	E1 01	4100		DW	CMDA
0217	E3	3550	XTHL	0267	43	4110		DB	'C'
0218	CA FA 01	3560	JZ	0268	91 02	4120		DW	CLEAR
021B	33	3570	INX	026A	42	4130		DB	'B'
021C	33	3580	INX	026B	A9 02	4140		DW	BLACK
021D	E3	3590	XTHL	026D	57	4150		DB	'W'
021E	3B	3600	DCX	026E	AF 02	4160		DW	WHITE
021F	3B	3610	DCX	0270	48	4170		DB	'H'
0220	E3	3620	XTHL	0271	B6 02	4180		DW	HOME
0221	C9	3630	RET	0273	4E	4190		DB	'N'
0222		3640	*	0274	BF 02	4200		DW	NORTH
0222	CD F6 01	3650	CMD09	0276	52	4210		DB	'R'
0225	78	3660	MOV	0277	C9 02	4220		DW	RIGHT
0226	B7	3670	ORA	0279	46	4230		DB	'F'
0227	C2 2E 02	3680	JNZ	027A	EB 02	4240		DW	FORWD
022A	F1	3690	POP	027C	18	4250		DB	18H
022B	C3 60 00	3700	JMP	027D	66 03	4260		DW	SAVE
022E		3710	*	027F	53	4262		DB	'S'
022E	E3	3720	ITER	0280	82 02	4264		DW	CMDS
022F	7C	3730	MOV	0282		4265	*		
0230	B5	3740	ORA	0282	CA 67 01	4266	CMDS	JZ	SKIP
0231	2B	3750	DCX	0285	3A F7 1F	4268		LDA	SFLAG
0232	C2 3E 02	3760	JNZ	0288	A7	4269		ANA	A
0235	E1	3770	POP	0289	3E 00	4270		MVI	A,0
0236	06 00	3780	MVI	028B	32 F7 1F	4272		STA	SFLAG
0238	CD 60 00	3790	CALL	028E	C3 7B 01	4274		JMP	TEST
023B	06 FF	3800	MVI	0291		4275	*		
023D	C9	3810	RET	0291	C8	4280	CLEAR	RZ	
023E		3820	*	0292	E5	4290		PUSH	H

SET FLAGS
RESET SFLAG

0325 2F
 0326 F5
 Rev. 1-2-83
 0327 B6
 0328 2F
 0329 32 F7 1F
 032C F1
 032D A6
 032E 77
 032F E1
 0330 C9
 0331
 0331 AF
 0332 D5
 0333 E1
 0334 B4
 0335 E6 01
 0337 29
 0338 B5
 0339 E6 03
 033B 6F
 033C AF
 033D B4
 033E E6 04
 0340 B5
 0341 EE 05
 0343 6F
 0344 AF
 0345 37
 0346 17
 0347 2D
 0348 F2 46 03
 034B F5
 034C 7A
 034D 1F
 034E 1F
 034F E6 3F
 0351 6F
 0352 7B
 0353 2F
 0354 D6 10
 0356 0F
 0357 0F
 0358 0F
 0359 F5
 035A E6 CO
 035C B5
 035D 6F
 035E F1
 035F E6 1F
 0361 C6 AO
 0363 67
 0364 F1
 0365 C9
 0366
 0366 21 00 04
 0369 11 00 DO

5520 CMA
 5522 PUSH PSW
 5524 ORA M
 5526 CMA
 5528 STA SFLAG
 5529 POP PSW
 5530 ANA M
 5540 MOV M,A
 5550 POP H
 5560 RET
 5570 *
 5580 ADR XRA A COMPUTE XY ADDRESS
 5590 PUSH D AND PROPER MASK BIT
 5600 POP H SCREEN ADDRESS IN HL
 5610 ORA H MASK IN A
 5620 ANI 1
 5630 DAD H
 5640 ORA L
 5650 ANI 3
 5660 MOV L,A
 5670 XRA A
 5680 ORA H
 5690 ANI 4
 5700 ORA L
 5710 XRI 5
 5720 MOV L,A
 5730 XRA A
 5740 STC
 5750 RAL
 5760 DCR L
 5770 JP \$-5
 5780 PUSH PSW
 5790 MOV A,D
 5800 RAR
 5810 RAR
 5820 ANI 63
 5830 MOV L,A
 5840 MOV A,E
 5850 CMA
 5860 SUI 16
 5870 RRC
 5880 RRC
 5890 RRC
 5900 PUSH PSW
 5910 ANI OCOH
 5920 ORA L
 5930 MOV L,A
 5940 POP PSW
 5950 ANI 31
 5960 ADI HRES
 5970 MOV H,A
 5980 POP PSW
 5990 RET
 5995 * SAVE MACROS FROM SCREEN
 6030 SAVE LXI H,MENU
 6040 LXI D,FLASH

036C 1A
 036D 77
 036E 23
 036F 13
 0370 7A
 0371 FE D4
 0373 C2 6C 03
 0376 3E 04
 0378 CD 98 CO
 037B C3 00 CO
 037E
 037E
 0400
 0800

SYMBOL TABLE

ADR 0331
 CD1 010B
 CMD 0060
 CMDLP 013B
 CMDT 0164
 D1 0034
 DIRCT 0031
 ERASE 0321
 FLSH 00D0
 G4 00B2
 HRES 00A0
 N1 01FA
 P2 01B3
 R1 02E0
 RNDB 0151
 SLOOP 036C
 TEST 017B
 X 1FF3

BLACK 02A9
 CD2 0113
 CMD09 0222
 CMDMS 01D3
 CNTLC CODC
 D2 0037
 DIS2 030D
 F1 00C4
 FORWD 02EB
 GETA 01F0
 I1 0018
 N2 0202
 P3 01C8
 R2 02E6
 SAVE 0366
 STACK 1FF0
 TWOD 01C6
 Y 1FF4

6050 SLOOP LDAX D
 6060 MOV M,A
 6070 INX H
 6080 INX D
 6090 MOV A,D
 6100 CPI FLSH+4
 6110 JNZ SLOOP
 6120 MVI A,4
 6130 CALL PTCN CLEAR SCREEN
 6140 JMP OCOOH MONITOR
 6142 *RESERVE BLOCK FOR SCREEN SAVE
 6144 ORG START+1024
 6148 MENU DS 1024
 6150 DANGR EQU \$+64

BORW 1FF2
 CD3 0134
 CMDA 01E1
 CMDPS 0193
 CPS1 01A7
 D3 0039
 DISP 02FB
 F2 00CE
 G1 009C
 GETCH 008D
 IT1 023E
 NORTH 02BF
 PLOT 0313
 RCMD 005D
 SEED 1FF0
 START 0000
 V1 00D8

C1 0071
 CL1 029A
 CMDBL 00F7
 CMDQM 0148
 CQ1 015D
 DANGR 0840
 DX 1FF5
 FIND 00B9
 G2 00A1
 HIRES A000
 ITER 022E
 NUMB 01F6
 PTCN C098
 RESRV 00D1
 SFLAG 1FF7
 T1 0189
 V2 00F1

C2 008B
 CLEAR 0291
 CMDD 00F8
 CMDS 0282
 CT1 016D
 DIGIT 00E7
 DY 1FF6
 FLASH D000
 G3 00B0
 HOME 02B6
 MENU 0400
 P1 01AA
 PUTA 01A8
 RIGHT 02C9
 SKIP 0167
 TABL 0249
 WHITE 02AF

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CC00      0010 ; CHARACTER GENERATOR AND
CC00      0020 ; DISPLAY PROGRAM FOR THE
CC00      0030 ; VECTOR GRAPHICS DISPLAY
CC00      0040 ;
CC00      0050 ; THIS LISTING CONTAINS A
CC00      0060 ; TEST & KEYBOARD ECHO
CC00      0070 ; ROUTINE STARTING AT
CC00      0080 ; LINE # 3980
CC00      0090 ;
CC00      0100 ; CTRL D, CLEAR SCREEN
CC00      0110 ; CTRL H, (08) BACKSPACE
CC00      0120 ; CTRL M, (0D) RETURN
CC00      0130 ;
CC00      0140 ; NOV 6,1977 * G.THURMOND
CC00      0150 ;
CC00      0160 ; DEFINITIONS & CONSTANTS
CC00      0170 ;
CC00      0180 BLOCK EQU 0A000H      HI RES BOARD
CC00      0190 BLOC EQU 0A0H
CC00      0200 KEYS EQU 0
CC00      0210 KEYD EQU 1
CC00      0220 KEYM EQU 40H
CC00      0230 MONIT EQU 0C000H
CC00      0240 ;
CC00      0250 ;
CC00      0260 ;
CC00 C3 95 CE      0270      JMP TEST
CC03      0280 CURS DS 2
CC05      0290 ;
CC05      0300 ; CHARACTER DISPLAY ROUTINE
CC05      0310 ;
CC05      0320 ; ENTER WITH ASCII CODE IN
CC05      0330 ; THE ACCUMULATOR.
CC05      0340 ; THIS ROUTINE DISPLAYS THE
CC05      0350 ; 64 CHARACTER ASCII UPPER
CC05      0360 ; CASE SET. IT WILL ACCEPT
CC05      0370 ; ALL ASCII CODES, BUT WILL
CC05      0380 ; WRITE THE LOWER CASE SET
CC05      0390 ; IN UPPER CASE.
CC05      0400 ;
CC05      0410 ;
CC05 E5      0420 DISPL PUSH H
CC06 D5      0430      PUSH D
CC07 C5      0440      PUSH B
CC08 F5      0450      PUSH PSW
CC09 21 FF 9F 0460      LXI H,BLOCK-1
CC0C FE 04 0470      CPI 4
CC0E CA 45 CC 0480      JZ CLEAR
CC11 2A 03 CC 0490      LHLD CURS
CC14 F5      0500      PUSH PSW
CC15 3E 20 0510      MVI A,' '
CC17 CD 63 CC 0520      CALL WRITE
CC1A F1      0530      POP PSW
CC1B FE 08 0540      CPI 8

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CC1D CA 54 CC      0550      JZ BS
CC20 FE 0D      0560      CPI ODH
CC22 CA 35 CC      0570      JZ SCROL
CC25 FE 20      0580      CPI 20H
CC27 DA 59 CC      0590      JC EXIT+3
CC2A CD 63 CC      0600      CALL WRITE
CC2D 23      0610      INX H
CC2E 23      0620      INX H
CC2F 7C      0630      MOV A,H
CC30 FE BE      0640      CPI BLOC+1EH
CC32 DA 56 CC      0650      JC EXIT
CC35 21 00 A0      0660 SCROL LXI H,BLOCK
CC38 01 80 A1      0670      LXI B,BLOCK+180H
CC3B 0A      0680 SCRL1 LDAX B
CC3C 77      0690      MOV M,A
CC3D 03      0700      INX B
CC3E 23      0710      INX H
CC3F 78      0720      MOV A,B
CC40 FE BE      0730      CPI BLOC+1EH
CC42 C2 3B CC      0740      JNZ SCRL1
CC45 23      0750 CLEAR INX H
CC46 7C      0760      MOV A,H
CC47 FE BE      0770      CPI BLOC+1EH
CC49 CA 51 CC      0780      JZ FINI
CC4C 36 00      0790      MVI M,0
CC4E C3 45 CC      0800      JMP CLEAR
CC51 21 C3 BD      0810 FINI LXI H,BLOCK+1DC3H
CC54 2B      0820 BS DCX H
CC55 2B      0830      DCX H
CC56 22 03 CC      0840 EXIT SHLD CURS
CC59 3E 5F      0850      MVI A,5FH
CC5B CD 63 CC      0860      CALL WRITE
CC5E F1      0870      POP PSW
CC5F C1      0880      POP B
CC60 D1      0890      POP D
CC61 E1      0900      POP H
CC62 C9      0910      RET
CC63      0920 ;
CC63      0930 ; WRITE CHARACTER
CC63      0940 ;
CC63      0950 ; ENTER THIS ROUTINE WITH
CC63      0960 ; LOWER LEFT CELL LOCATION
CC63      0970 ; IN H & L, AND THE ASCII
CC63      0980 ; CODE IN THE ACCUMULATOR.
CC63      0990 ;
CC63 F5      1000 WRITE PUSH PSW
CC64 C5      1010      PUSH B
CC65 D5      1020      PUSH D
CC66 E5      1030      PUSH H
CC67 FE 60      1040      CPI 60H
CC69 DA 6E CC      1050      JC $+2
CC6C E6 5F      1060      ANI 5FH
CC6E 26 00      1070      MVI H,0
CC70 6F      1080      MOV L,A
CC71 29      1090      DAD H
CC72 29      1100      DAD H

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CC73 29
 CC74 11 94 CB
 CC77 19
 CC78 E3
 CC79 11 00 FF
 CC7C 19
 CC7D D1
 CC7E 01 3F 00
 CC81 3E 04
 CC83 F5
 CC84 09
 CC85 13
 CC86 1A
 CC87 77
 CC88 23
 CC89 13
 CC8A 1A
 CC8B 77
 CC8C F1
 CC8D 3D
 CC8E C2 83 CC
 CC91 D1
 CC92 C1
 CC93 F1
 CC94 C9
 CC95
 CC95
 CC95
 CC95
 CC95
 CC95
 CC95 00 00
 CC97 00 00
 CC99 00 00
 CC9B 00 00
 CC9D 0A 00
 CC9F 0A 00
 CCA1 08 00
 CCA3 08 00
 CCA5 55 00
 CCA7 44 00
 CCA9 00 00
 CCAB 00 00
 CCAD 55 00
 CCAF DD 80
 CCB1 DD 80
 CCB3 44 00
 CCB5 1B 20
 CCB7 9B 00
 CCB9 3B 80
 CCBB 08 00
 CCBD F0 20
 CCBF 06 00
 CCC1 61 20
 CCC3 04 80
 CCC5 62 00

1110 DAD H
 1120 LXI D,CHTAB-101H
 1130 DAD D
 1140 XTHL
 1150 LXI D,-100H
 1160 DAD D
 1170 POP D
 1180 LXI B,3FH
 1190 MVI A,4
 1200 CELL PUSH PSW
 1210 DAD B
 1220 INX D
 1230 LDAX D
 1240 MOV M,A
 1250 INX H
 1260 INX D
 1270 LDAX D
 1280 MOV M,A
 1290 POP PSW
 1300 DCR A
 1310 JNZ CELL
 1320 POP D
 1330 POP B
 1340 POP PSW
 1350 RET
 1360 ;
 1370 ; 64 CHARACTER VERSION
 1380 ; ASCII TO 5X7 CHARACTER
 1390 ; DATA TABLE.
 1400 ;
 1410 ;
 1420 CHTAB DW 0 SP
 1430 DW 0
 1440 DW 0
 1450 DW 0
 1460 DW 0AH !
 1470 DW 0AH
 1480 DW 8
 1490 DW 8
 1500 DW 55H "
 1510 DW 44H
 1520 DW 0
 1530 DW 0
 1540 DW 55H #
 1550 DW 80DDH
 1560 DW 80DDH
 1570 DW 44H
 1580 DW 201BH \$
 1590 DW 9BH
 1600 DW 803BH
 1610 DW 8
 1620 DW 20F0H %
 1630 DW 6
 1640 DW 2061H
 1650 DW 8004H
 1660 DW 62H &

CCC7 98 00
 CCC9 A9 80
 CCCB 48 80
 CCCD 0A 00
 CCCF 08 00
 CCD1 00 00
 CCD3 00 00
 CCD5 18 00
 CCD7 A0 00
 CCD9 90 00
 CCDB 08 00
 CCDD 09 00
 CCDF 00 A0
 CCE1 01 80
 CCE3 08 00
 CCE5 2A 20
 CCE7 4E 00
 CCE9 6E 20
 CCEB 08 00
 CCED 02 00
 CCEF 3B 20
 CCF1 0A 00
 CCF3 00 00
 CCF5 00 00
 CCF7 00 00
 CCF9 0A 00
 CCFB 40 00
 CCFD 00 00
 CCFF 33 20
 CD01 00 00
 CD03 00 00
 CD05 00 00
 CD07 00 00
 CD09 00 00
 CD0B 08 00
 CD0D 00 20
 CD0F 06 00
 CD11 60 00
 CD13 00 00
 CD15 6C 20
 CD17 A6 A0
 CD19 E0 A0
 CD1B 4C 00
 CD1D 1A 00
 CD1F 0A 00
 CD21 0A 00
 CD23 4C 00
 CD25 6C 20
 CD27 03 80
 CD29 60 00
 CD2B CC 80
 CD2D CC A0
 CD2F 07 00
 CD31 20 A0
 CD33 4C 00
 CD35 07 00

1670
 1680
 1690
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 1800
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 2220

DW 98H
 DW 80A9H
 DW 8048H
 DW 0AH
 DW 8
 DW 0
 DW 0
 DW 18H
 DW 0A0H
 DW 90H
 DW 8
 DW 9
 DW 0A000H
 DW 8001H
 DW 8
 DW 202AH
 DW 4EH
 DW 206EH
 DW 8
 DW 2
 DW 203BH
 DW 0AH
 DW 0
 DW 0
 DW 0
 DW 0AH
 DW 40H
 DW 0
 DW 2033H
 DW 0
 DW 0
 DW 0
 DW 0
 DW 8
 DW 2000H
 DW 6
 DW 60H
 DW 0
 DW 206CH
 DW 0A0A6H
 DW 0A0E0H
 DW 4CH
 DW 1AH
 DW 0AH
 DW 0AH
 DW 4CH
 DW 206CH
 DW 8003H
 DW 60H
 DW 80CCH
 DW 0A0CCH
 DW 7
 DW 0A020H
 DW 4CH
 DW 7

0
 1
 2
 3
 4

CD37	65	00	2230	DW	65H		CDA7	B3	80	2790	DW	80B3H
CD39	CD	80	2240	DW	80CDH		CDA9	A0	A0	2800	DW	0A0A0H
CD3B	04	00	2250	DW	4		CDAB	CC	00	2810	DW	0CCH
CD3D	EC	80	2260	DW	80ECH	5	CDAD	6C	20	2820	DW	206CH
CD3F	CC	20	2270	DW	20CCH		CDAF	A0	00	2830	DW	0A0H
CD41	20	A0	2280	DW	0A020H		CDB1	A0	20	2840	DW	20A0H
CD43	4C	00	2290	DW	4CH		CDB3	4C	00	2850	DW	4CH
CD45	1C	80	2300	DW	801CH	6	CDB5	EC	20	2860	DW	20ECH
CD47	B3	00	2310	DW	0B3H		CDB7	A0	A0	2870	DW	0A0A0H
CD49	A0	A0	2320	DW	0A0A0H		CDB9	A0	A0	2880	DW	0A0A0H
CD4B	4C	00	2330	DW	4CH		CDBB	CC	00	2890	DW	0CCH
CD4D	CC	A0	2340	DW	0A0CCH	7	CDBD	EC	80	2900	DW	80ECH
CD4F	06	00	2350	DW	6		CDBF	B3	00	2910	DW	0B3H
CD51	50	00	2360	DW	50H		CDC1	A0	00	2920	DW	0A0H
CD53	40	00	2370	DW	40H		CDC3	CC	80	2930	DW	80CCH
CD55	6C	20	2380	DW	206CH	8	CDC5	EC	80	2940	DW	80ECH
CD57	93	80	2390	DW	8093H		CDC7	B3	00	2950	DW	0B3H
CD59	A0	A0	2400	DW	0A0A0H		CDC9	A0	00	2960	DW	0A0H
CD5B	4C	00	2410	DW	4CH		CDCB	80	00	2970	DW	80H
CD5D	6C	20	2420	DW	206CH	9	CDCD	6C	80	2980	DW	806CH
CD5F	93	A0	2430	DW	0A093H		CDCF	A0	00	2990	DW	0A0H
CD61	01	80	2440	DW	8001H		CDD1	A4	A0	3000	DW	0A0A4H
CD63	C8	00	2450	DW	0C8H		CDD3	4C	80	3010	DW	804CH
CD65	00	00	2460	DW	0	:	CDD5	A0	A0	3020	DW	0A0A0H
CD67	08	00	2470	DW	8		CDD7	B3	A0	3030	DW	0A0B3H
CD69	08	00	2480	DW	8		CDD9	A0	A0	3040	DW	0A0A0H
CD6B	00	00	2490	DW	0		Cddb	80	80	3050	DW	8080H
CD6D	00	00	2500	DW	0	;	CDDD	4E	00	3060	DW	4EH
CD6F	08	00	2510	DW	8		CDDF	0A	00	3070	DW	0AH
CD71	0A	00	2520	DW	0AH		CDE1	0A	00	3080	DW	0AH
CD73	40	00	2530	DW	40H		CDE3	4C	00	3090	DW	4CH
CD75	06	00	2540	DW	6	<	CDE5	00	A0	3100	DW	0A000H
CD77	60	00	2550	DW	60H		CDE7	00	A0	3110	DW	0A000H
CD79	42	00	2560	DW	42H		CDE9	20	A0	3120	DW	0A020H
CD7B	04	00	2570	DW	4		CDEB	4C	00	3130	DW	4CH
CD7D	00	00	2580	DW	0	=	CDED	A1	80	3140	DW	80A1H
CD7F	CC	80	2590	DW	80CCH		CDEF	B8	00	3150	DW	0B8H
CD81	CC	80	2600	DW	80CCH		CDF1	A9	00	3160	DW	0A9H
CD83	00	00	2610	DW	0		CDF3	80	80	3170	DW	8080H
CD85	42	00	2620	DW	42H	>	CDF5	A0	00	3180	DW	0A0H
CD87	04	20	2630	DW	2004H		CDF7	A0	00	3190	DW	0A0H
CD89	06	00	2640	DW	6		CDF9	A0	00	3200	DW	0A0H
CD8B	40	00	2650	DW	40H		CDFB	CC	80	3210	DW	80CCH
CD8D	6C	20	2660	DW	206CH	?	CDFD	B1	A0	3220	DW	0A0B1H
CD8F	06	00	2670	DW	6		CDFE	AA	A0	3230	DW	0A0AAH
CD91	08	00	2680	DW	8		CE01	A0	A0	3240	DW	0A0A0H
CD93	08	00	2690	DW	8		CE03	80	80	3250	DW	8080H
CD95	6C	20	2700	DW	206CH	e	CE05	A0	A0	3260	DW	0A0A0H
CD97	AB	A0	2710	DW	0A0ABH		CE07	E2	A0	3270	DW	0A0E2H
CD99	AC	00	2720	DW	0ACH		CE09	A4	A0	3280	DW	0A0A4H
CD9B	4C	80	2730	DW	804CH		CE0B	80	80	3290	DW	8080H
CD9D	19	00	2740	DW	19H	A	CE0D	6C	20	3300	DW	206CH
CD9F	A0	A0	2750	DW	0A0A0H		CE0F	A0	A0	3310	DW	0A0A0H
CDA1	EC	A0	2760	DW	0A0ECH		CE11	A0	A0	3320	DW	0A0A0H
CDA3	80	80	2770	DW	8080H		CE13	4C	00	3330	DW	4CH
CDA5	EC	20	2780	DW	20ECH	B	CE15	EC	20	3340	DW	20ECH

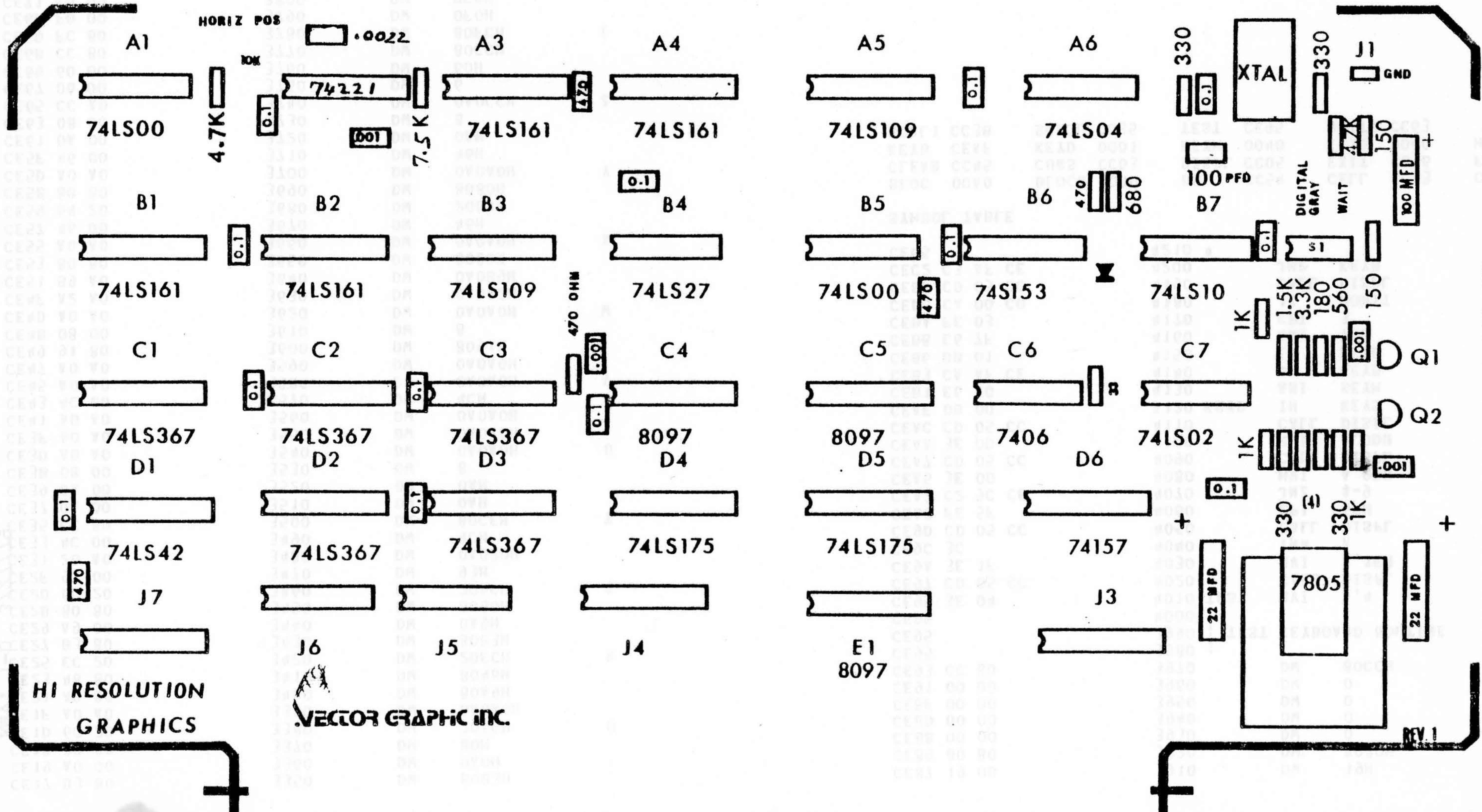
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Rev. 1-2-B
3/2/79

CE17 B3 80	3350	DW	80B3H		CE87 19 00	3910	DW	19H	
CE19 A0 00	3360	DW	0A0H		CE89 80 80	3920	DW	8080H	
CE1B 80 00	3370	DW	80H		CE8B 00 00	3930	DW	0	
CE1D 6C 20	3380	DW	206CH	Q	CE8D 00 00	3940	DW	0	
CE1F A0 A0	3390	DW	0A0A0H		CE8F 00 00	3950	DW	0	
CE21 A9 80	3400	DW	80A9H		CE91 00 00	3960	DW	0	
CE23 48 80	3410	DW	8048H		CE93 CC 80	3970	DW	80CCH	
CE25 EC 20	3420	DW	20ECH	R	CE95	3980			
CE27 B3 80	3430	DW	80B3H		CE95	3990	; TEST KEYBOARD ROUTINE		
CE29 A9 00	3440	DW	0A9H		CE95	4000			
CE2B 80 80	3450	DW	8080H		CE95 3E 04	4010	TEST	MVI	A,4
CE2D 6C 20	3460	DW	206CH	S	CE97 CD 05 CC	4020		CALL	DISPL
CE2F 93 00	3470	DW	93H		CE9A 3E 1F	4030		MVI	A,1FH
CE31 20 A0	3480	DW	0A020H		CE9C 3C	4040		INR	A
CE33 4C 00	3490	DW	4CH		CE9D CD 05 CC	4050		CALL	DISPL
CE35 CE 80	3500	DW	80CEH	T	CEA0 FE 5F	4060		CPI	5FH
CE37 0A 00	3510	DW	0AH		CEA2 C2 9C CE	4070		JNZ	\$-9
CE39 0A 00	3520	DW	0AH		CEA5 3E 0D	4080		MVI	A,0DH
CE3B 08 00	3530	DW	8		CEA7 CD 05 CC	4090		CALL	DISPL
CE3D A0 A0	3540	DW	0A0A0H	U	CEAA 3E 0D	4100		MVI	A,0DH
CE3F A0 A0	3550	DW	0A0A0H		CEAC CD 05 CC	4110		CALL	DISPL
CE41 A0 A0	3560	DW	0A0A0H		CEAF DB 00	4120	KEYB	IN	KEYS
CE43 4C 00	3570	DW	4CH		CEB1 E6 40	4130		ANI	KEYM
CE45 A0 A0	3580	DW	0A0A0H	V	CEB3 CA AF CE	4140		JZ	KEYB
CE47 A0 A0	3590	DW	0A0A0H		CEB6 DB 01	4150		IN	KEYD
CE49 91 80	3600	DW	8091H		CEB8 E6 7F	4160		ANI	7FH
CE4B 08 00	3610	DW	8		CEBA FE 03	4170		CPI	3
CE4D A0 A0	3620	DW	0A0A0H	W	CEBC CA 00 CO	4180		JZ	MONIT
CE4F A2 A0	3630	DW	0A0A2H		CEBF CD 05 CC	4190		CALL	DISPL
CE51 B9 A0	3640	DW	0A0B9H		CEC2 C3 AF CE	4200		JMP	KEYB
CE53 80 80	3650	DW	8080H		CEC5	4210			
CE55 A0 A0	3660	DW	0A0A0H	X					
CE57 46 00	3670	DW	46H						
CE59 64 20	3680	DW	2064H						
CE5B 80 80	3690	DW	8080H						
CE5D A0 A0	3700	DW	0A0A0H	Y					
CE5F 46 00	3710	DW	46H						
CE61 0A 00	3720	DW	0AH						
CE63 08 00	3730	DW	8						
CE65 CC A0	3740	DW	0A0CCH	Z					
CE67 06 00	3750	DW	6						
CE69 60 00	3760	DW	60H						
CE6B CC 80	3770	DW	80CCH						
CE6D FC 80	3780	DW	80FCH	[
CE6F F0 00	3790	DW	0F0H						
CE71 F0 00	3800	DW	0F0H						
CE73 CC 80	3810	DW	80CCH						
CE75 20 00	3820	DW	20H	\					
CE77 42 00	3830	DW	42H						
CE79 04 20	3840	DW	2004H						
CE7B 00 00	3850	DW	0						
CE7D CD A0	3860	DW	0A0CDH]					
CE7F 05 A0	3870	DW	0A005H						
CE81 05 A0	3880	DW	0A005H						
CE83 CC 80	3890	DW	80CCH						
CE85 00 00	3900	DW	0						

SYMBOL TABLE

BLOC	00A0	BLOCK	A000	BS	CC54	CELL	CC83	CHTAB
CLEAR	CC45	CURS	CC03	DISPL	CC05	EXIT	CC56	FINI
KEYB	CEAF	KEYD	0001	KEYM	0040	KEYS	0000	MONIT
SCRL1	CC3B	SCROL	CC35	TEST	CE95	WRITE	CC63	



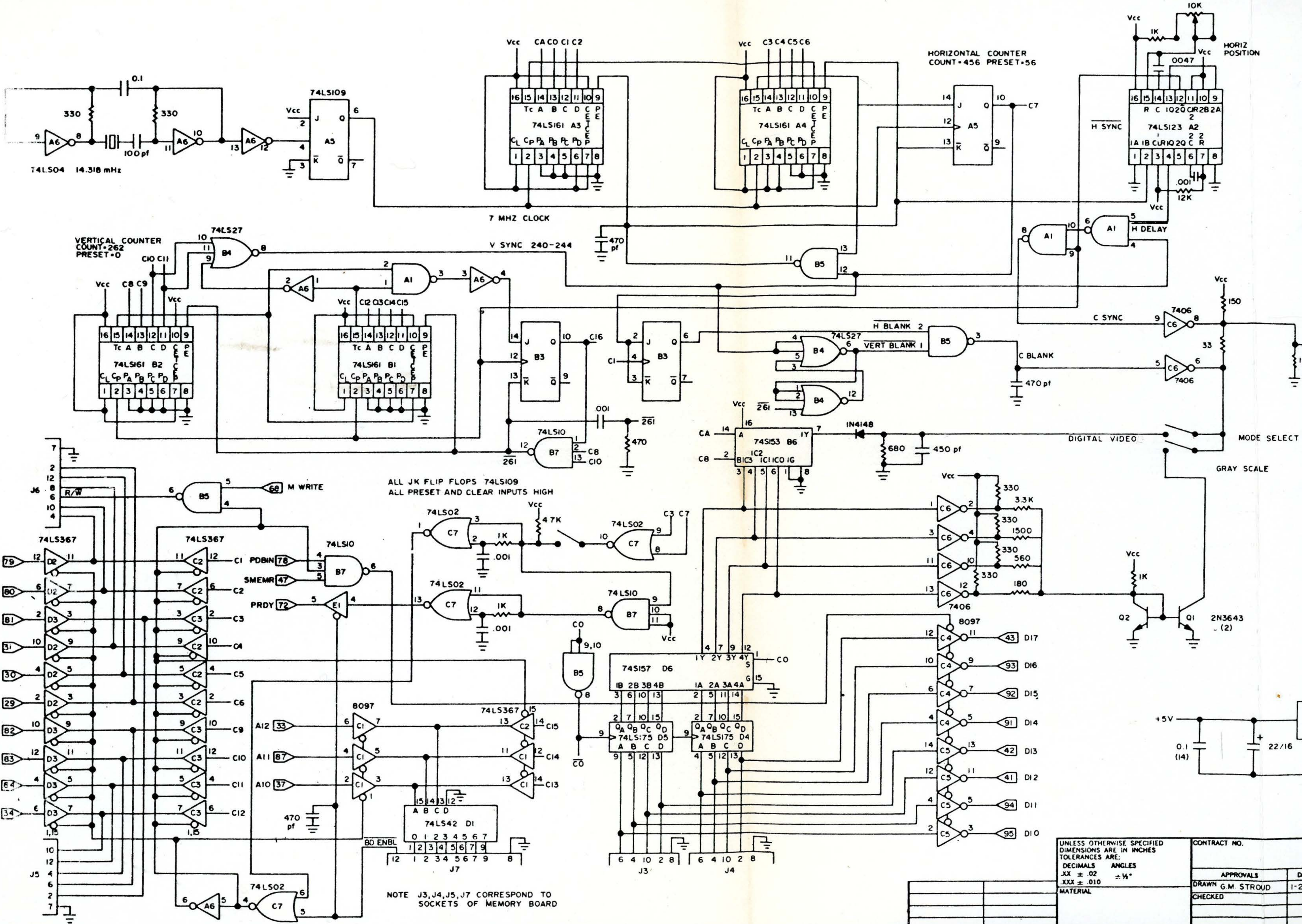
HI RESOLUTION GRAPHICS

VECTOR GRAPHIC INC.

High Resolution Graphics Board Users Manual

SCHEMATIC ERRATA

1. The 8097 bus driver shown on the lower right side of the schematic is NOT an inverter.
2. A2, shown on the upper right hand corner of the schematic, should be a 74221.
3. The capacitor connected to pin 14 of A2 is .0022 Mf.
4. The resistor connected to pin 16 of A2 is 4.7K.
5. The resistor connected to pin 7 of A2 is 7.5K.

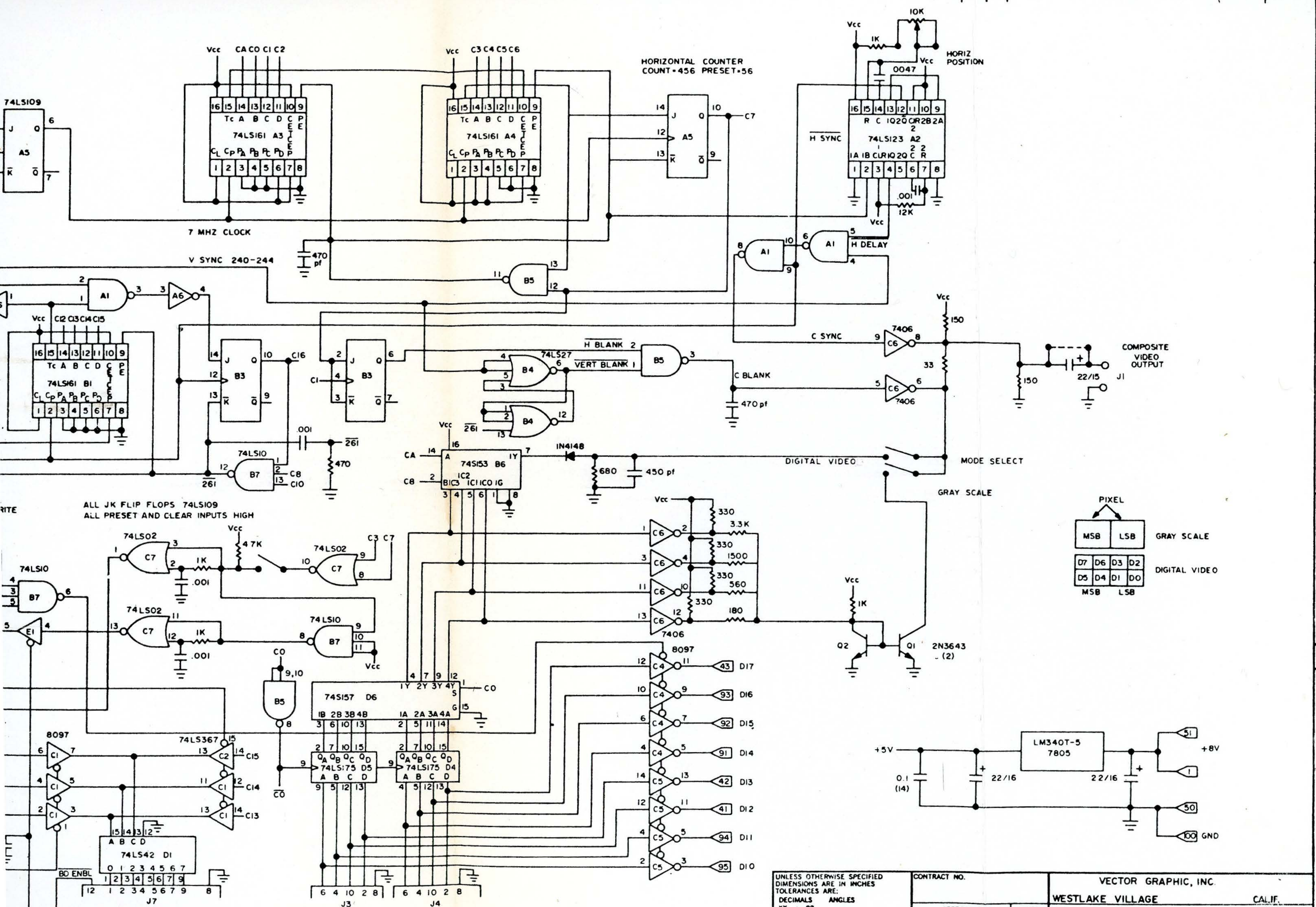


ALL JK FLIP FLOPS 74LS109
ALL PRESET AND CLEAR INPUTS HIGH

NOTE J3, J4, J5, J7 CORRESPOND TO
SOCKETS OF MEMORY BOARD

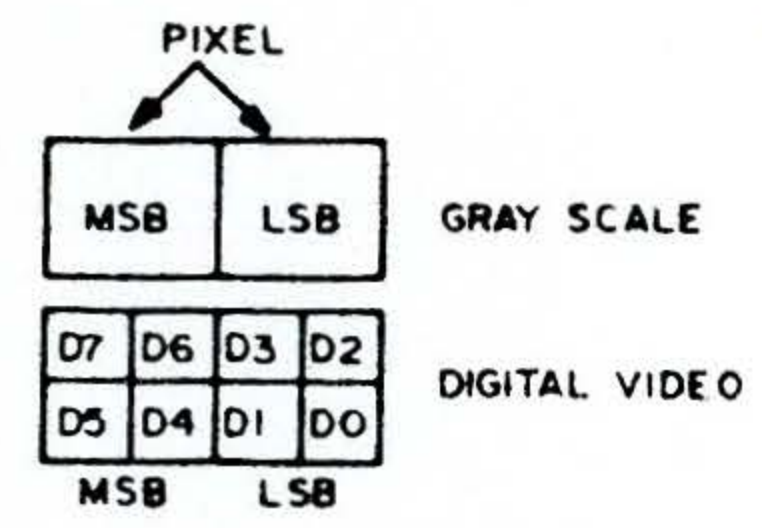
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS .XX ± .02 .XXX ± .010		CONTRACT NO.	
MATERIAL		APPROVALS	DATE
FINISH		DRAWN G.M. STROUD	1-25
NEXT ASSY		CHECKED	
USED ON			

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ALL JK FLIP FLOPS 74LS109
ALL PRESET AND CLEAR INPUTS HIGH

NOTE J3, J4, J5, J7 CORRESPOND TO SOCKETS OF MEMORY BOARD



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS ANGLES .XX ± .02 ± 1/2° .XXX ± .010	CONTRACT NO.		VECTOR GRAPHIC, INC.	
	APPROVALS		WESTLAKE VILLAGE CALIF.	
	DRAWN G.M. STROUD		DATE 1-25-77	
	CHECKED		HIGH RESOLUTION GRAPHIC DISPLAY	
MATERIAL	FINISH		SIZE CODE IDENT NO. DRAWING NO.	