Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface (see figure 1).

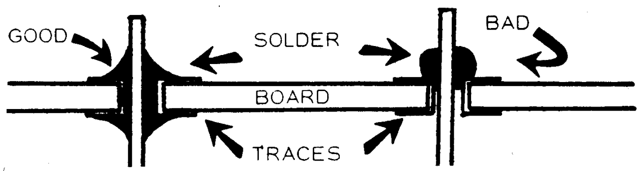


Figure 1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty) it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking, don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without over heating.

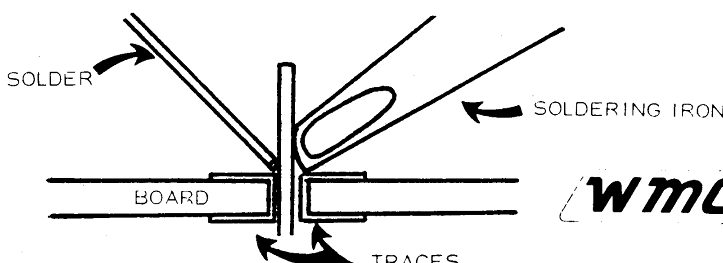


Figure 2.

WMC/inc.

The CPU-1 is designed to operate with the S100 (**WAMECO**) bus (see figure 3A, B). There are 19 pins not otherwise used in this bus. These pins are available for non-standard configurations. It is advisable to carefully consider any modification since this will limit board usage to a modified system.

Parts List

C1, C2, C18	3	33µf tantalum electrolytic capacitor
C3, C6, C8, C10-17, C24, C26	13	0.1 µf 50V ceramic disc capacitor
C4, C5, C7, C9	4	22µf 50V axial electrolytic capacitor
C19, C25	2	470 pf 50V ceramic disc capacitor
C20, C23	2	47pf 50V ceramic disc capacitor
*C21	1	3-27pf variable capacitor
C22	1	0.01 50V ceramic disc capacitor
D1	1	1N751 zener 5V diode
D2	1	1N4148 silicon diode
*L1	1	2µh inductor
R1	1	620Ω 1/2 W resistor
**R2-7, R11-39, R48	36	2.7 KΩ 1/4 W resistor
R8	1	10KΩ 1/4 W resistor
R9, R10	2	220Ω 1/4 W resistor
R4-R47	8	4.7 KΩ 1/4 W resistor
V1, V23	2	7805 or 340T0-5 +5V regulator
**V2	1	8214
V3	1	8080A
**V4, V5	2	8212
**V6	1	74LS30
V7	1	74L00
V8	1	8224
V9, V10, V16-V22	9	DM 8097/74367 or 8T97
**V11, V14, V15	3	DM 8098/74368 or 8T98
V12	1	74L S32
V13	1	7812
V24	1	74LS74
V25	1	74LS02
X1	1	18 MHz crystal
	1	40 pin socket
	3	24 pin sockets
	13	16 pin sockets
	5	14 pin sockets
	3	heatsinks
	3	6-32X3/4" screws and nuts

* used in optional circuit if frequency of crystal is off.

** V2, V4, V6, V11, V12, R18-31 are used for vector interrupt circuit. If this circuit is not being used, do not install.

S-1ØØ (WAMECO) BUS STRUCTURE

PIN	MNEMONIC	TERM.
1	+5V	
2	+15V	
3	XRDY	X
4	VIØ	X
5	VI1	X
6	VI2	X
7	VI3	X
8	VI4	X
9	VI5	X
10	VI6	X
11	VI7	X
12		
13		
14		
15		
16		
17		
18	STAT DISABLE	X
19	CIC DISABLE	X
20	UNPROTECT	X
21	SS	X
22	ADDR DSBL	X
23	DO DSBL	X
24	Ø2	X
25	Ø1	X
26	PHLDA	X
27	PWAIT	
28	PINTE	
29	A5	
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	DO1	X
36	DOØ	X
37	A10	
38	DO4	X
39	DO5	X
40	DO6	X
41	DI2	X
42	DI3	X
43	DI7	X
44	SMI	
45	SOUT	
46	SINP	
47	SMEMR	
48	SHLTA	
49	CLOCK (2MHz)	
50	GND	

PIN	MNEMONIC	ALTER. PIN DESIG.	TERM.
51	+5V	A	
52	-15V	B	
53	SSW DSB	C	
54	EXT CLR	D	X
55		E	
56		F	
57		H	
58		J	
59		K	
60		L	
61		M	
62		N	
63		P	
64		R	
65		S	
66		T	
67	PHANTOM	U	X
68	MWRITE	V	X
69	PS	W	
70	PROTECT	X	X
71	RUN	Y	X
72	PRDY	Z	X
73	PINT	a	X
74	PHOLD	b	X
75	PRESET	c	X
76	PSYNC	d	X
77	PWR	e	X
78	PDBIN	f	X
79	AØ	h	
80	A1	j	
81	A2	k	
82	A6	l	
83	A7	m	
84	A8	n	
85	A13	p	
86	A14	r	
87	A11	s	
88	DO2	t	X
89	DO3	u	X
90	DO7	v	X
91	DI4	w	X
92	DI5	x	X
93	DI6	y	X
94	DI1	z	X
95	DIØ	AA	X
96	SINTA	AB	
97	SWO	AC	
98	SSTACK	AD	
99	POC	AE	
100	GND	AF	

Figure 3A

S-100 (WAMECO) BUS DESCRIPTION

Pin #	Mnemonic	Enabled State	Description
1	+8 Volts	NA	Unregulated +8 Volts DC. This voltage should not be less than +8 or greater than +11 volts.
2	+16 Volts	NA	Unregulated +16 Volts DC. This voltage should not be less than +16 or greater than +20 Volts.
3	XRDY	Low	Causes CPU to enter WAIT state when enabled.
4	$\overline{\text{VI0}}$	Low	Vectored Interrupt priority 0
5	$\overline{\text{VI1}}$	Low	Vectored Interrupt priority 1
6	$\overline{\text{VI2}}$	Low	Vectored Interrupt priority 2
7	$\overline{\text{VI3}}$	Low	Vectored Interrupt priority 3
8	$\overline{\text{VI4}}$	Low	Vectored Interrupt priority 4
9	$\overline{\text{VI5}}$	Low	Vectored Interrupt priority 5
10	$\overline{\text{VI6}}$	Low	Vectored Interrupt priority 6
11	$\overline{\text{VI7}}$	Low	Vectored Interrupt priority 7
12	---	NA	Not used
13	---	NA	Not used
14	---	NA	Not used
15	---	NA	Not used
16	---	NA	Not used
17	---	NA	Not used
18	STAT DISABLE	Low	The eight status line buffers on the CPU board enter the high impedance state when enabled.
19	C/C DISABLE	Low	The six command/control line buffers on the CPU board enter the high impedance state when enabled.
20	UNPROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be cleared.
21	SS	High	Indicates the CPU is single stepping.
22	$\overline{\text{ADDR DSBL}}$	Low	The 16 address line buffers on the CPU board enter the high impedance state when enabled.
23	$\overline{\text{DO DSBL}}$	Low	The eight data-out lines on the CPU board enter the high impedance state when enabled.
24	Ø 2	High	Buffered TTL CPU phase 2 clock.
25	Ø 1	High	Buffered TTL CPU phase 1 clock.
26	PHLDA	High	CPU board "Hold Acknowledge" to HOLD-H input.
27	PWAIT	High	CPU output showing a WAIT state is occuring.

Figure 3B.

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
28	PINTE	High	CPU output showing that Interrupts are enabled.
29	A5	High	Address Bit 5
30	A4	High	Address Bit 4
31	A3	High	Address Bit 3
32	A15	High	Address Bit 15
33	A12	High	Address Bit 12
34	A9	High	Address Bit 9
35	DO1	High	CPU Data Out Bit 1
36	DO0	High	CPU Data Out Bit 0
37	A10	High	Address Bit 10
38	DO4	High	CPU Data Out Bit 4
39	DO5	High	CPU Data Out Bit 5
40	DO6	High	CPU Data Out Bit 6
41	DI2	High	Data In Bit 2 to CPU
42	DI3	High	Data In Bit 3 to CPU
43	DI7	High	Data In Bit 7 to CPU
44	SM1	High	CPU output indicating it is performing Fetch Instruction
45	SOUT	High	CPU output showing it is in a output cycle.
46	SINP	High	CPU output showing it is in a input cycle.
47	SMEMR	High	CPU status signal indicating the current cycle is a Memory Read cycle.
48	SHLTA	High	CPU status signal indicating the CPU is halted.
49	CLOCK(2MHz)	Low	A buffered 2 MHz clock for general use.
50	GND	NA	Ground (common)
51	+8 Volts	NA	(Same as pin 1)
52	-16 Volts	NA	Unregulated-16 Volts DC. This voltage should not be greater than -16 or less than -20 Volts.
53	$\overline{\text{SSW DSB}}$	Low	Sense Switch Disable disables CPU board data input buffers so that CPU can read sense switches.
54	$\overline{\text{EXT CLR}}$	Low	Front panel generated I/O clear signal.
55	---	NA	Not used
56	---	NA	Not used
57	---	NA	Not used
58	---	NA	Not used
59	---	NA	Not used
60	---	NA	Not used
61	---	NA	Not used
62	---	NA	Not used
63	---	NA	Not used
64	---	NA	Not used
65	---	NA	Not used
66	---	NA	Not used
67	**PHANTOM**	NA	**Used for Memory Bank Selection (or for Sol$_c$ System)**

Figure 3B (continued)

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
68	MWRITE	High	CPU output showing Data Out Bus data is to be written into the memory selected by the address lines.
69	$\overline{PS}$	Low	Shows Protect Status of selected memory.
70	PROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be set.
71	RUN	High	Front panel indication that CPU run instruction has been input.
72	PRDY	Low	Causes the CPU to enter the WAIT state when enabled.
73	$\overline{PINT}$	Low	If interrupts have been enabled causes the CPU to enter the Interrupt Acknowledge condition at the conclusion of the current instruction.
74	$\overline{PHOLD}$	Low	CPU input which causes a HOLD status to occur. DMA transfer request signal is $\overline{PHOLD}$.
75	$\overline{PRESET}$	Low	CPU board system reset signal.
76	PSYNC	High	CPU output showing the start of a new machine cycle. This signal is used on the CPU board to enable the loading of the System Status Latch.
77	$\overline{PWR}$	Low	Indication that data on the Data Out Bus is to be written either to a memory or an I/O device.
78	PDBIN	Low	Indication to the selected memory or I/O device that the CPU expects data on the Data In Bus.
79	A0	High	Address Bit 0
80	A1	High	Address Bit 1
81	A2	High	Address Bit 2
82	A6	High	Address Bit 6
83	A7	High	Address Bit 7
84	A8	High	Address Bit 8
85	A13	High	Address Bit 13
86	A14	High	Address Bit 14
87	A11	High	Address Bit 11
88	DO2	High	CPU Data Out Bit 2
89	DO3	High	CPU Data Out Bit 3
90	DO7	High	CPU Data Out Bit 7
91	DI4	High	Data In Bit 4 to CPU
92	DI5	High	Data In Bit 5 to CPU
93	DI6	High	Data In Bit 6 to CPU

Figure 3B (continued)

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
94	DI1	High	Data In Bit 1 to CPU
95	DI0	High	Data In Bit 0 to CPU
96	SINTA	High	CPU Interrupt Acknowledge Signal
97	SWO	Low	CPU output indicating the current cycle involves writing to a memory or I/O device.
98	SSTACK	High	CPU output indicating the address bus contains the stack address and the curre[nt] cycle will have a stack operation.
99	$\overline{\text{POC}}$	Low	Power On Clear reset signal
100	GND	NA	Ground (common)

Figure 3B (continued)

Tools and Supplies Needed to Assemble and Test CPU-1

1 Q Tip cotton swab
1 pair needle nosed pliers
1 pair diagonal cutting pliers
1 bottle rosin flux
1 tube silicone thermal heat grease
1 jar solder cleaner
1 roll solder wick
1 phillips screwdriver
1 small adjustable wrench or socket to fit regulator nuts
1 roll (.031" or .040") SN60/40 rosin core solder
1 25-to 40 Watt soldering iron with small spade tip
1 strong light
1 magnifying glass
1 Xacto knife
1 multimeter
1 variable 15V power supply

I Assembly of CPU-1

I-1. Before placing any parts on the board, check the board for any hairline shorts (slivers). All boards have been inspected at least three times before shipping. Still, a good hobbyist checks any board he buys.

I-2. Using a strong light and a magnifying glass, very carefully check all leads on the top of the board (this is the side marked CPU-1). If any slivers are found, carefully cut and scrape them with an Xacto knife. The underside of the board will be checked after assembly.

I-3. Place all the 14 and 16 pin sockets in their positions on the top side of the board.

I-4. After positioning all sockets in place, put a book or other flat stiff object on top of the sockets. Hold the book tight against the board and turn them over so that the underside of the board is up. Press down on the board and solder one pin on each end of each socket. This will ensure the sockets are flat against the board. When tacking all sockets is completed, finish soldering all the other pins of the sockets.

NOTE

DO NOT PUT IC'S IN SOCKETS AT THIS TIME. THEY WILL BE INSTALLED LATER.

I-5. Bend the leads on R2-7, R11-39, R48(2. 7KΩ RED, VIOLET, RED) and place in board. Check parts placement drawing (figure 4) for correct locations. Bend the leads on the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

I-6. Bend the leads on R40-47 (4.7KΩ YELLOW, VIOLET, RED) and place in board. Check parts placement drawing (figure 4) for correct locations. Bend the leads on the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

I-7. Bend the leads on R1 (620Ω BLUE, RED, BROWN), R8 (10KΩ BROWN, BLACK, ORANGE), R9, R10 (220Ω RED, RED, BROWN) and place in board. Check parts placement drawing (figure 4) for correct locations. Bend the leads on the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

CAUTION

CHECK DISC CAPACITORS FOR PROPER VALUE BEFORE INSERTING IN BOARD. ENSURE .01μF AND .1 μF DISC CAPACITORS ARE NOT INTERCHANGED.

I-8. Put the leads of C3, C6, C8, C10-C17, C24, C26 (.1μf) disc capacitors in the board. Check parts location drawing (figure 4) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder all the capacitors. Clip the leads flush with the underside of the board with the diagonal pliers.

I-9. Put the leads of C19, C25(470pf), C22(.01μf), C20, C23 (47pP) in the board. Check parts location drawing (figure 4) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder all the capacitors. Clip the leads flush with the underside of the board with the diagonal pliers.

I-10. Place C4, C5, C7, C9 (22μf axial electrolytics), C1, C2, C18 (33μf tantalum electrolytics) in place. Ensure that the polarities are correct. Check parts placement drawing (figure 4) for correct placement and polarity. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder the capacitors in place. Clip the leads flush with the underside of the board with the diagonal pliers.

I-11. Place D1 (1N751 five volt zener) and D2 (1N148) in place. Ensure that the polarities are correct. Check parts placement drawing (figure 4) for correct placement and polarity. Bend the leads of the diodes to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder the diodes in place. Clip the leads flush with the underside of the board with the diagonal pliers.

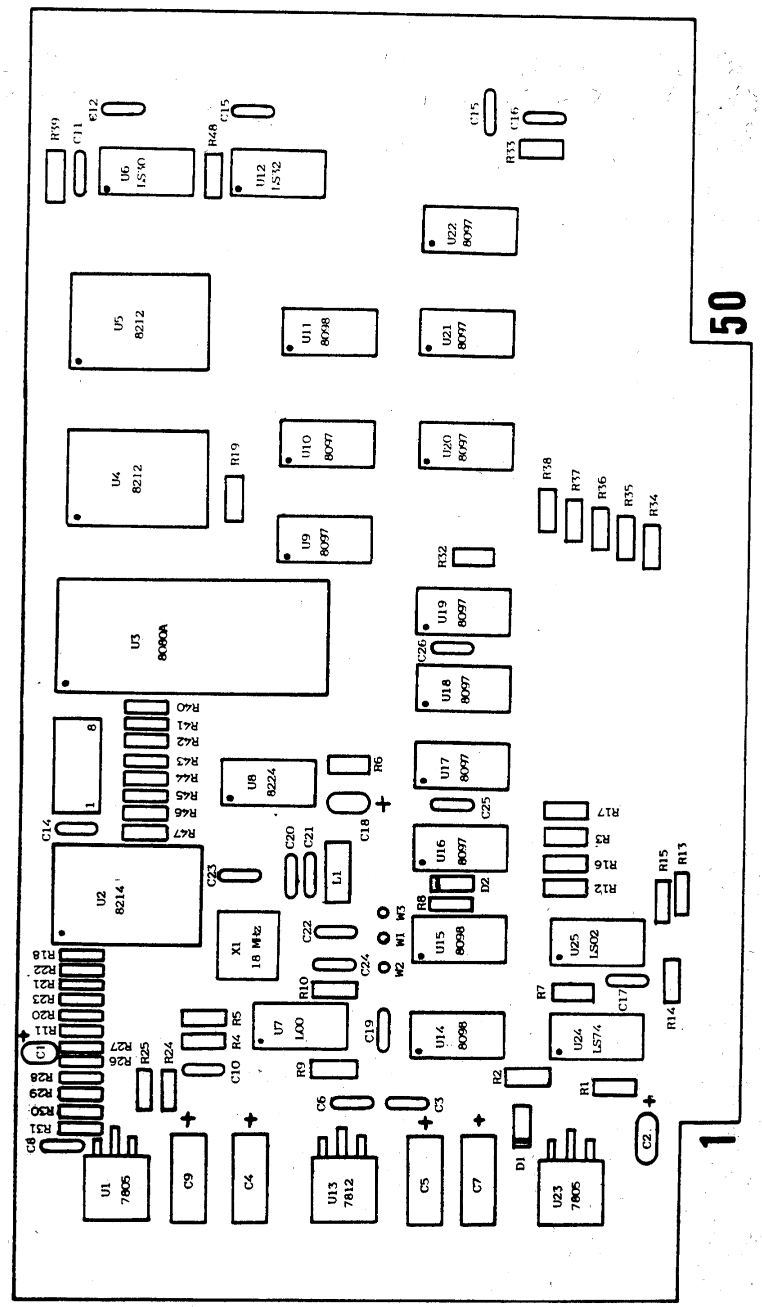
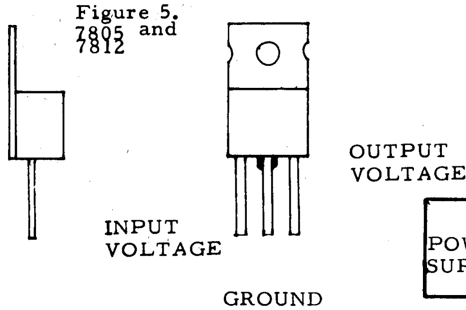


Figure 4. CPU-1 Parts Placement Diagram

I-12. Place X1 (18 MHz crystal) in place. It is recommended that the leads be bent so that the crystal will be close to the board. If the crystal is to be placed so that it will be close to the board, wrap the crystal with a layer of plastic insulation tape so that no shorting of traces will occur. Ensure that the polarity is correct. Check parts placement drawing (figure 4) for correct placement and polarity. Bend the leads of the crystal to retain it in place until it is soldered. Turn the board over and rest it on books as before. Solder the crystal in place. Clip the leads flush with the underside of the board with the diagonal pliers.

I-13. Before installing the 7805 five volt regulators and 7812 twelve volt regulator, it is recommended that they be tested for proper voltage regulation.

Figure 5. 7805 and 7812



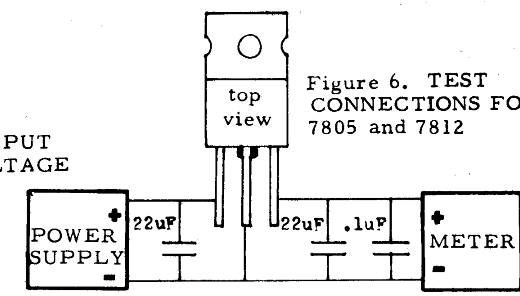


Figure 6. TEST CONNECTIONS FOR 7805 and 7812

To prevent oscillation of the regulators, assemble a test rig as shown. The capacitors must be installed observing correct polarity. This test rig is for pre-installation testing only. The filter capacitors installed on the board serve the same purpose in the final assembly.

Attach the power supply and multimeter leads to the 7805 or 7812 as shown in figure 6. Place the multimeter in a DC range that will allow 10 volts to be displayed. The regulators need a 2.0 volt minimum difference between the input voltage and the regulated output voltage. If the power supply has a voltmeter, observe the input voltage during the test. If the power supply does not have a voltmeter, switch the + meter lead between the output lead and the input lead of the regulator. The input and regulated voltages can then be observed.

I-14. Slowly increase the input voltage and observe the output voltage. When the input voltage is between 7.0 and 7.5 volts, the regulated output of a properly operating 78 05 should be between 4.8 and 5.2 volts. When the input voltage is between 14.0 and 14.5 volts, the regulated output of a properly operating 7812 should be between 11.8 and 12.2 volts. Replace any regulator that does not meet these limits.

I-15. When the regulators have been tested as outlined in I-14, place the regulators on the board so that the mounting hole on the regulator lines up with the corresponding hole on the CPU-1. Check parts placement drawing (figure 4) for the correct placement of the regulators. Note where the leads on the regulators pass over the connection holes on the CPU-1. Bend the leads on the regulators so that the leads can be inserted into the proper holes. Mount the regulators on the board using a #6 nut and 5/8" 6-30 screw. Insert a heatsink between the board and the 7805. Solder the leads of the 7805's in place.

I-16. Remove the nuts and screws from the regulators. Bend the regulators upward and remove the heatsinks. Place a moderate amount of silicone thermal heat grease on the underside of the regulators and the underside of the heatsinks with a Q tip cotton swab. Coat all of the area mentioned with an even coating of the heat grease. Reinstall the heatsinks, nuts, and screw. Ensure the nuts are tight.

I-17. If the CPU-1 is to be operated without the vector interrupt capability, place a shorting wire between W1 and W2. V2, V4, V6, V11 and V12 do not need to be installed. In this configuration the CPU-1 will operate with a standard S-100 system (ie., IMSAI, ALTAIR).

I-18. If the CPU-1 is to be operated with the vector interrupt capability, place a shorting wire between W1 and W3 and install V2, V4, V6, V11 and V23. Read the explanation on the interrupt circuit operation at the end of section II.

I-19. Clean off the flux on the underside of the board with flux cleaner.

II. Inspection and Testing

II-1. Use a bright light and magnifying glass to inspect all the traces on the underside of the board. If any slivers are found, cut and scrape them with an Xacto knife. Use the solder wick and soldering iron to remove any solder bridges found. Cover the solder bridge with flux and place a clean piece of solder wick on top of the bridge. Place the soldering iron on top of the solder wick and hold until solder is seen flowing up into the solder wick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

NOTE

AT THIS TIME NO IC'S HAVE BEEN INSTALLED ON THE BOARD. DO NOT INSTALL IC'S ON THE BOARD UNTIL CALLED FOR IN THE CHECK OUT PROCEDURE.

From PIN	Resistance	To PIN
1	Short	51
2	----	
3	2.7K	1
4	2.7K	1
5	2.7K	1
6	2.7K	1
7	2.7K	1
8	2.7K	1
9	2.7K	1
10	2.7K	1
11	2.7K	1
12	----	
13	----	
14	----	
15	----	
16	----	
17	----	
18	2.7K	1
19	2.7K	1
20	----	
21	----	
22	2.7K	1
23	2.7K	1
24	----	
25	----	
26	----	
27	----	
28	----	
29	----	
30	----	
31	----	
32	----	
33	----	
34	----	
35	----	
36	----	
37	----	
38	----	
39	----	
40	----	
41	2.7K	1
42	2.7K	1
43	2.7K	1
44	----	
45	----	
46	----	
47	----	
48	----	
49	----	
50	Short	100

From PIN	Resistance	To PIN
51	Short	1
52	----	
53	----	
54	----	
55	----	
56	----	
57	----	
58	----	
59	----	
60	----	
61	----	
62	----	
63	----	
64	----	
65	----	
66	----	
67	----	
68	----	
69	----	
70	----	
71	----	
72	2.7K	1
73	2.7K	1
74	2.7K	1
75	2.7K	1
76	----	
77	----	
78	----	
79	----	
80	----	
81	----	
82	----	
83	----	
84	----	
85	----	
86	----	
87	----	
88	----	
89	----	
90	----	
91	2.7K	1
92	2.7K	1
93	2.7K	1
94	2.7K	1
95	2.7K	1
96	----	
97	----	
98	----	
99	----	
100	Short	50

Figure 7.

II-2. Place the multimeter in the R x 1 scale. Place one probe on the gold finger for pin 1. Place the other probe on all the other fingers sequentially to check for shorts. Repeat this procedure for each pin. There should be only two sets of pins that are shorted; 1 to 51 and 50 to 100. There are 25 pins that will read 2.7 K of resistance (figure 7). If any other pair of pins are shorted, use a strong light and magnifying glass to locate the solder bridge or sliver causing the short. When the short has been located, correct it as outlined in II-1. If there is no solder bridge or sliver, a component is shorted, check the CPU-1 schematic (figure 8) to locate the probable component. Lift one lead of the suspected component and recheck between the two fingers that had a bad reading. If the bad reading is now correct, replace the component. If the reading is still bad, continue troubleshooting until the faulty component is located and replaced. Ensure all components that had a lead lifted have the lead reconnected.

WARNING

DO NOT INSTALL OR REMOVE ANY BOARD IN COMPUTER WITH POWER ON. DAMAGE TO BOARDS AND COMPUTER MAY RESULT.

II-3. Ensure computer is OFF. Plug the CPU-1 into the motherboard. Check that CPU-1 is correctly plugged in and the board is fully seated in the connector. Turn computer power ON and check outputs of all three regulators on CPU-1. If any regulator does not have an output voltage as stated in I-14, turn computer power OFF and replace defective regulator. Repeat II-3 until all regulator voltages are good. If voltages are good, turn computer power OFF and remove CPU-1 from mother board.

II-4. Install all IC's on CPU-1. Check parts placement drawing (see figure 4) for proper location and correct polarity of IC's.

CAUTION

ENSURE ALL IC'S ARE INSTALLED CORRECTLY. INCORRECT POLARIZATION OF IC WILL RESULT IN DAMAGE TO IC AND CAUSE SUBSEQUENT TROUBLES TO APPEAR ON BOARD.

II-5. Ensure computer is OFF. Plug the CPU-1 into the motherboard. Check that CPU-1 is correctly plugged in and the board is fully seated in the connector. Install the plug connecting the front panel board to the CPU-1. The CPU-1 is designed so that it will work in an IMSAI computer. If the CPU-1 is not to be used in an IMSAI, configure the plug so that it will match the CPU-1 design.

NOTE

WHEN POWER IS APPLIED TO AN 8080 SYSTEM, THE MICROPROCESSOR DOES NOT COME UP IN ANY DETERMINABLE MODE. TO CORRECTLY INITIALIZE THE COMPUTER, HOLD THE STOP SWITCH IN STOP AND PUSH THE RESET SWITCH TO RESET.

II-6. The computer has to have at least one memory board installed. One has to be addressed 0000H.

II-7. Apply power to the computer. If PROTECT lamp illuminates, place the PROTECT/UNPROTECT switch in UNPROTECT.

II-8. Place all address switches OFF (down).

II-9. MI, MO, WAIT and MEMR lights should be on. The data in location 0000 will also be displayed.

II-10. Check each address switch and lamp for proper operation by turning on each one singly and then placing the EXAMINE switch to EXAMINE. The lamp for the appropriate switch should illuminate.

II-11. Place all address switches down, hold the RESET switch in RESET. All address lights should illuminate and the status lamps should be extinguished.

II-12. Actuate the EXAMINE NEXT switch a number of times and observe the address lamps. If the switch is working correctly, the address lamps will increment from 0000.

II-13. Momentarily actuate the RESET switch, then actuate the DEPOSIT NEXT a number of times and observe the address lamps. If the switch is working correctly, the address lamps will increment from 0000.

II-14. Momentarily actuate the RESET switch, then check each data switch and lamp for proper operation by turning on each one singly and then placing the EXAMINE switch to EXAMINE. The lamp for the appropriate switch should illuminate.

II-15. When everything has checked out to this point, the computer is ready to run a test program. Remember to momentarily actuate RESET after the program is loaded so the program will start from 0000. Before running the program, step through a portion of the program using the SINGLE STEP switch. This will check out the SINGLE STEP function. Check the data in each memory location while single stepping by actuating the EXAMINE function.

II-16. Actuate the RESET switch, then run the test program by actuating the RUN switch.

<u>III Vector Interrupt</u>

III-1. If vector interrupt capability is not desired, place a shorting wire between W1 and W2. Refer to parts placement diagram (figure 4) for location of shorting wire.

III-2. To select vector interrupt, place the shorting wire between W1 and W3.

III-3. The vectored interrupt circuitry allows programmed operation to be interrupted with processing continuing at predetermined locations in main memory. There are eight locations that may be vectored to, depending on the interrupt request.

III-4. To generate an interrupt , the $\overline{PINT}$ line and a vectored interrupt line must be pulled down at the same time. The eight VI lines correspond to the following locations (in hex) for the 8080A:

Interrupt	Location	Priority
VI0	38	lowest
VI1	30	
VI2	28	
VI3	20	
VI4	18	
VI5	10	
VI6	8	
VI7	0	highest

Table 1. Interrupts and Priorities

III-5. The interrupt priority circuitry must be programmed before proper operation can occur. This is accomplished by sending I/O data to the 8214 interrupt chip on the CPU board. The I/O device code is BF (HEX). There are nine levels of interrupt priorities that may be programmed.

III-6. In each level of interrupt only the priority interrupt equivalent to that level or a higher priority interrupt may generate an interrupt to the 8080. The data in table 2 programs the interrupt level and priority level that is accepted by the 8080.

LEVEL	INTERRUPT(S) ALLOWED	BIT3	BIT2	BIT1	BIT0	REMARKS
0	NONE	0	0	0	0	See note 1
1	VI 7 only	0	0	0	1	
2	VI 6 and higher	0	0	1	0	
3	VI 5 and higher	0	0	1	1	
4	VI 4 and higher	0	1	0	0	
5	VI 3 and higher	0	1	0	1	
6	VI 2 and higher	0	1	1	0	
7	VI 1 and higher	0	1	1	1	
8	all	1	X	X	X	See note 2

Table 2. Interrupt levels and BIT data

Note 1. Priority level is programmed by bits 0, 1, 2.

Note 2. Priority level masking is disabled and straight 8 level priority takes place.

III-7. Program Example 1.

OUT BF ; assume accumulator "A" has 04 data in it.

This command will program the interrupt circuitry is set so that any interrupt that has a priority lower than 4 cannot interrupt the processor.

III-8. Program Example 2.

OUT BF ; Assume accumulator "A" has 0C in it.

This command programs the interrupt circuitry so that there are 8 levels of priority with no masking of lower levels.

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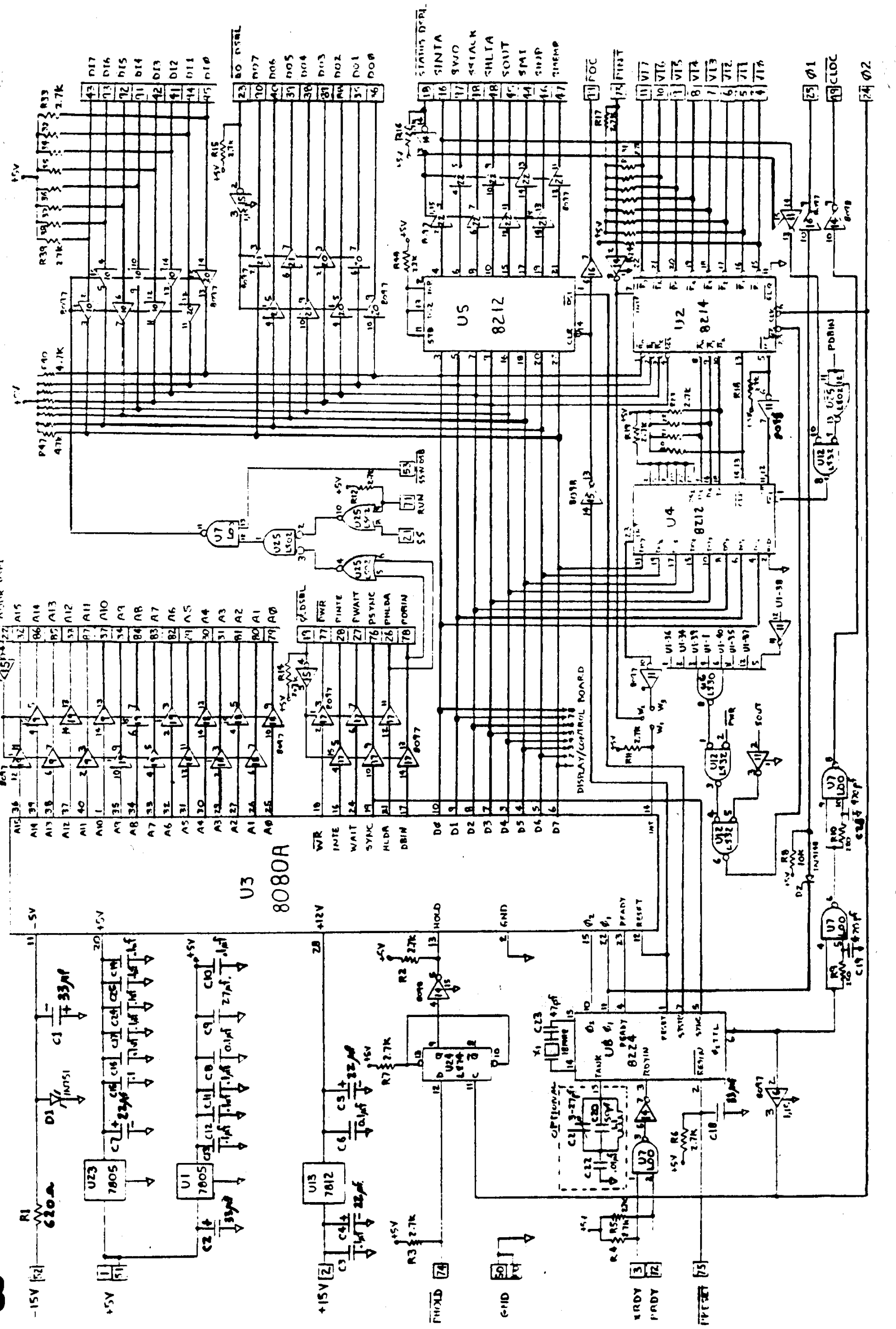

Figure 8. CPU-1 Schematic

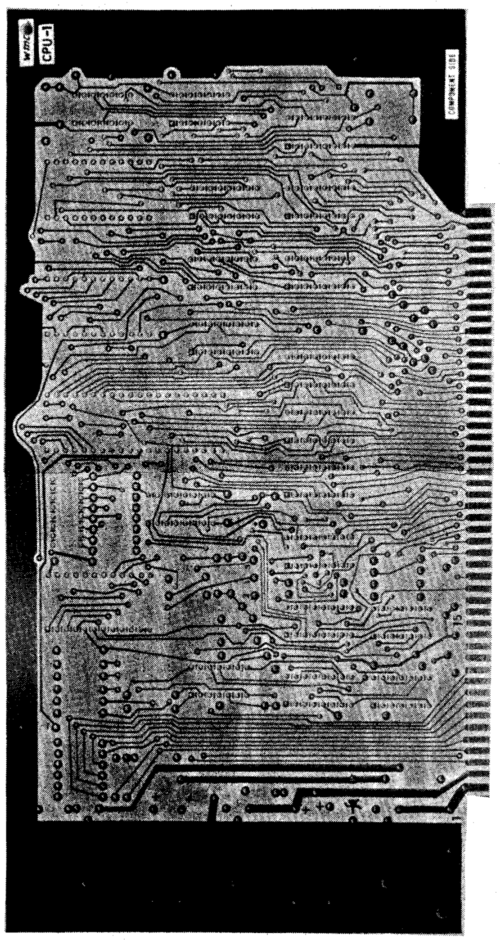

Figure 9A. COMPONENT SIDE OF CPU-1

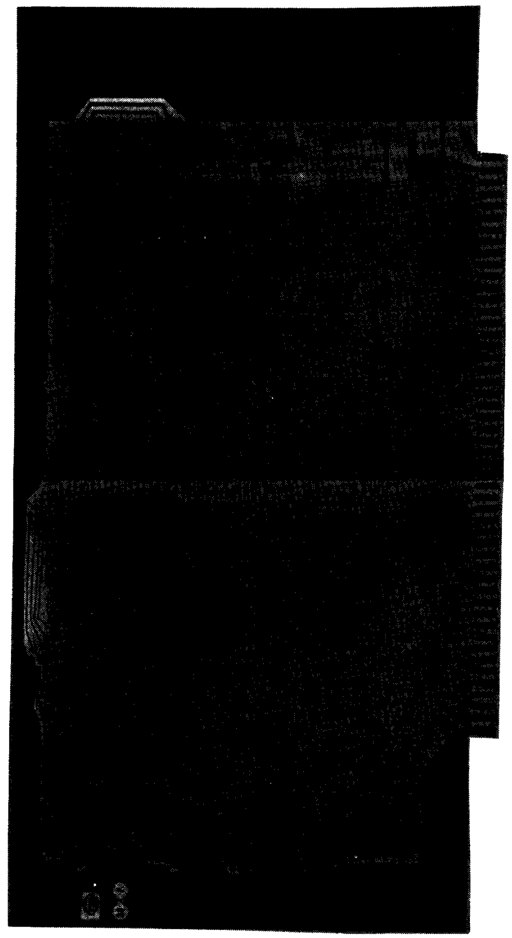

Figure 9B. NONCOMPONENT SIDE OF CPU-1