

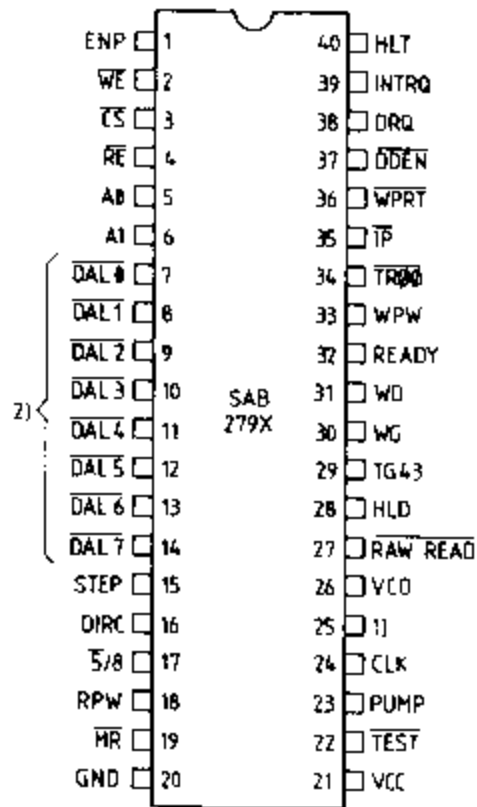
SIEMENS

SAB 279X Floppy Disk Formatter/Controller Family

Features	SAB 2791	SAB 2793	SAB 2795	SAB 2797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Output			X	X
Internal CLK Divide	X	X		

- On-Chip PLL Data Separator
- On-Chip Write Precompensation Logic
- Single +5V Supply
- Accommodates Single and Double Density Formats
- IBM 3740 Single Density (FM)
- IBM System 34 Double Density (MFM)
- Automatic Seek with Verify
- Multiple Sector Read Write
- TTL Compatible
- Programable Control
- Selectable Track-to-Track Access
- Head Load Timing
- Software Compatible with the SAB 179X Floppy Disk Formatter/Controller Family
- Soft Sector Format Compatibility

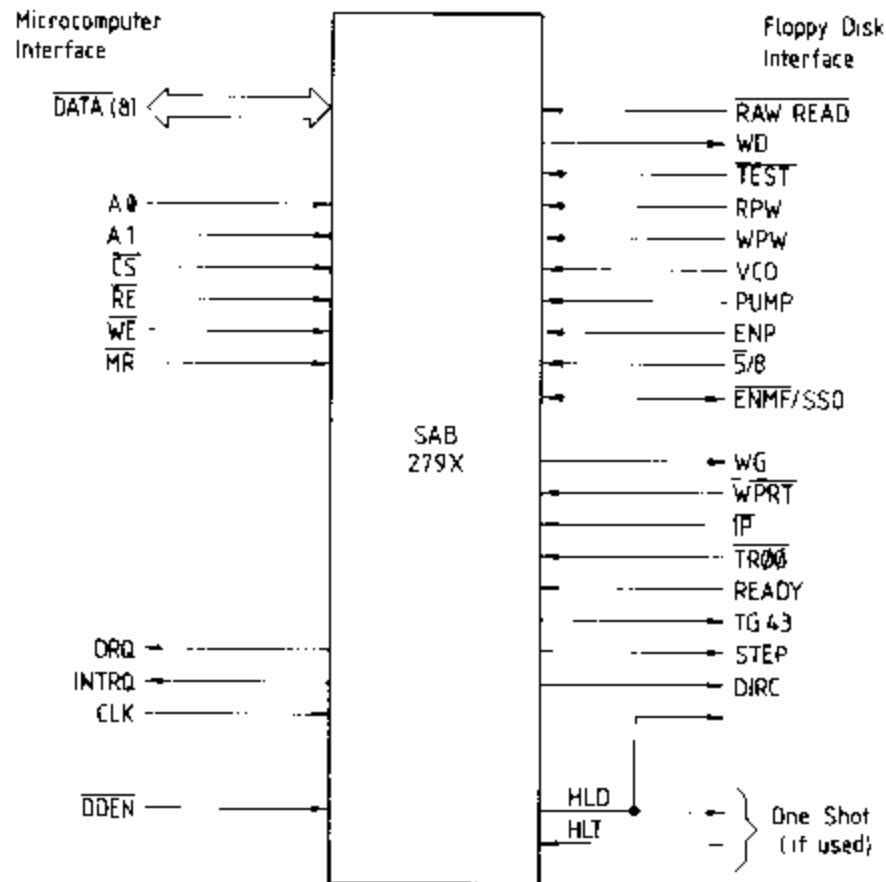
Pin Connections



1) SAB 2791/2793 = ENMF
SAB 2795/2797 = SS0

2) SAB 2793/2797 = True Bus

Logic Diagram



SAB 279X is a floppy disk controller family of N-channel MOS LSI components designed to interface with SAB 8080/8085/8086/8051 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems. Software compatible with its predecessor, the SAB 179X, the device also contains a high performance Phase- Lock-Loop Data Separator as well as Write Precompensation Logic. When operating in Double Density Mode,

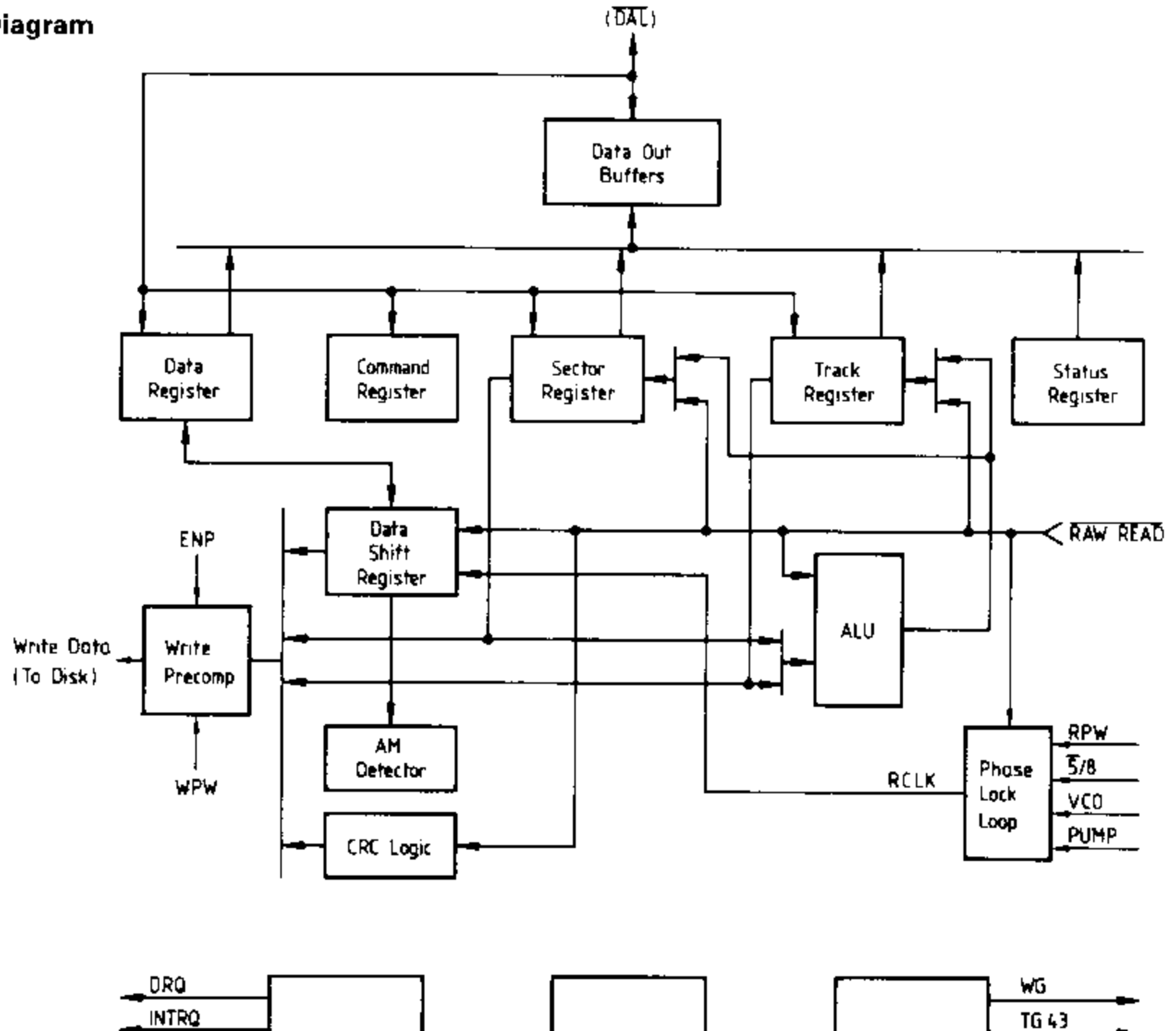
Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼"-8" Floppy Disk and Micro Floppy Disk interface.

ENP	1	I	ENABLE PRECOMP- A logic high on this input enables write precompensation to be performed on the Write Data output																									
WE	2	I	WRITE ENABLE- A logic low on this input gates data on the DAL into the selected register when CS is low																									
CS	3	I	CHIP SELECT- A logic low on this input selects the chip and enables computer communication with the device																									
RE	4	I	READ ENABLE- A logic low on this input controls the placement of data from a selected register on the DAL when CS is low																									
A0, A1	5,6	I/O	REGISTER SELECT LINES- These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: <table><tr><td>CS</td><td>A1</td><td>A0</td><td>RE</td><td>WE</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Status Register</td><td>Command Register</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Track Register</td><td>Track Register</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Sector Register</td><td>Sector Register</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Data Register</td><td>Data Register</td></tr></table>	CS	A1	A0	RE	WE	0	0	0	Status Register	Command Register	0	0	1	Track Register	Track Register	0	1	0	Sector Register	Sector Register	0	1	1	Data Register	Data Register
CS	A1	A0	RE	WE																								
0	0	0	Status Register	Command Register																								
0	0	1	Track Register	Track Register																								
0	1	0	Sector Register	Sector Register																								
0	1	1	Data Register	Data Register																								
DAL0 to DAL7	7-14	I/O	DATA ACCESS LINES- Eight bit bidirectional bus used for transfer of commands, status and data. These lines are inverted on SAB2791 and SAB2795																									
STEP	15	O	STEP- The step output contains a pulse for each step																									
DIRC	16	O	DIRECTION- Direction output is active high when stepping in, active low when stepping out																									
58	17	I	5¼",8" SELECT- This input selects the internal VCC frequency for use with 5¼" drives or 8" drives																									
RPW	18	I	READ PULSE WIDTH- An external potentiometer tied to this input controls the phase comparator within the data separator																									
MR	19	I	MASTER RESET- A logic low (50usec min.) on this input resets the device and loads hex03(?) into the command register. The Not Ready bit (Status bit 7) is reset during MR active. When MR is brought to a logic high a Restore command is executed, regardless of the state of the Ready signal from the drive. Also hex 01 is loaded into Sector Register.																									
TEST	22	I	TEST- A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins																									

PUMP	23	O	PUMP- High-impedance output signal which is forced high or low to increase/decrease the VCO frequency
CLK	24	I	CLOCK- This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz +- 1% for 8" drives, 1 MHz +1% for mini-floppies
ENMF	25	I	ENABLE MINI-FLOPPY(SAB2791/2793)- A logic low on this input enables an internal divide by 2 of the master clock.This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 7 MHz clock on Pin 24, this line must be left open or tied to a logic 1
SSD	25	O	SIDE SELECT OUTPUT(SAB2795/2797)- The logic level of the Side Select output is directly controlled by the U flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector ID field. If they do not compare, Status Bit4 (RNF) is set. The Side Select output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a master reset condition
VCO	26	-	VOLTAGE CONTROLLED OSCILLATOR- An external capacitor tied to this pin adjusts the VCO center frequency
RAWREAD	27	I	RAW READ- The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition
HLD	28	O	HEAD LOAD- The HLD output controls the loading ofthe Read/Write head against the media
TG43	29	O	TRACK GREATER THAN 43- This output informs the drive that the Read/Write head is positioned between tracks 44 and 76. This output is valid only during read and write commands
WG	30	O	WRITE GATE- This output is made valid before writing is to be performed on the diskette
WD	31	O	WRITE DATA- MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats
READY	32	I	READY- This input indicates disk readiness and is sampled for a logic high before read or write commands are performed. If Ready is low the read or write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7
WPW	33	I	WRITE PRECOMP WIDTH- An external potentiometer tied to this input controls the amount of delay in write precompensation mode
TR00	34	I	TRACK 00- This input informs the SAB 279X that the Read/Write head is positioned over Track 00
IP	35	I	INDEX PULSE- This input informs the SAB 279X when the index hole is encountered on the diskette

WPRT	36	I	WRITE PROTECT- This input is sampled whenever a write command is received. A logic low terminates the command and sets the Write Protect status bit
DDEN	37	I	DOUBLE DENSITY- This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected
DRQ	38	O	DATA REQUEST- This output indicates that the Data Register contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the computer through reading or loading the Data Register
INTRQ	39	O	INTERRUPT REQUEST- This output is set at the completion of any command and is reset when the Status Register is read or the Command Register is written to
HLT	40	I	HEAD LOAD TIMING- When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a single shot triggered by HLD
VCC	21	-	POWER SUPPLY(+5V)
VSS	20	-	GROUND(0V)

Block Diagram



General Description

The SAB 279X are N-channel MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The SAB 279X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The SAB 279X contains all the features of its predecessor, the SAB 179X, plus a high performance phase-lock-loop data separator as well as write precompensation logic. In double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the SAB 179X and SAB 279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical in each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The SAB 279X is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The SAB 2793 is identical with the SAB 2791, except that the DAL lines are true for systems that utilize true data busses. The SAB 2795/7 has a side select output for controlling double sided drives.

Organisation

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register (DSR) - This 8-bit register assembles serial data from the Read Data input (RAW READ) during read operations and transfers serial data to the Write Data output during write operations.

Data Register (DR) - This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk write operations information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired track position. This register is loaded from the DAL and gated on to the DAL under processor control.

Track Register (TR) - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt command. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC includes all information starting with the address mark up to the CRC character. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrements and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control - All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector - The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation - enables write precompensation to be performed on the Write Data output.

Data Separator - a high performance phase-lock-loop data separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer data, status, and control words out of, or into the SAB 279X. The DAL are three state buffers that are enabled as

output drivers when Chip Select (-CS) and Read Enable(-RE)are active (low logic state) or act as input receivers when -CS and Write Enable (-WE) are active.

When transfer or data with the Floppy Disk Controller is required by the host processor, the device address is decoded and -CS is made low. The address bits A1 and A0, combined with the signals -RE during a read operation or -WE during a write operation are interpreted as selector for the following registers:

A1	A0	READ	WRITE
\$	\$	Status Register	Command Register
\$	1	Track Register	Track Register
1	\$	Sector Register	Sector Register
1	1	Data Register	Data Register

During direct memory access (DMA) types of data are transferred between the Data Register of the SAB 279X and the processor. the Data Request (DRQ) output is used in data transfer control. This signal also appears as status bit 1 during read and write operations.

In disk read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters have been lost by having transferred new data into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

In disk write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

Upon completion of every command an INTRQ is generated, INTRQ is reset either by reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a force Interrupt command condition is met.

The SAB 279X has two modes of operation depending on the state of -DDEN (Pin 37). When -DDEN = 1, Single Density (FM) is selected. When -DDEN = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the SAB 2791/2793, the -ENMF input (Pin25) can be used for controlling both, 5¼" and 8" drives with a single 2 MHz clock. When -ENMF = 0, an internal divide by 2 of the CLK is performed. When -ENMF = 1, no divide takes place. This allows the use of a 2 MHz clock for both, 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The -5/8 input (Pin 17) is used to select data separator operation by internally dividing the read clock. When -5/8 = 0, 5¼" data separation is selected; when -5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	-ENMF (25)	-5/8 (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

All other conditions are invalid.

Functional Description

The SAB 279X is software compatible with the SAB 179X series of floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the SAB 179X can be transferred to a SAB 279X system without modification.

In addition to the SAB 179X, the SAB 219X contains an internal data separator and write precompensation circuit. The TEST (Pin 22) line is used to adjust both, data separator and precompensation. When -TEST = 0, the WD (Pin 31) line is internally connected to the output of the write precomp single shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second single shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.

Similarly, data separation is also adjusted with -TEST = 0. The TG43 (Pin 29) line is internally connected to the output of the read data single shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the read clock output (500 kHz for 8" drives). The VCO trimming capacitor (Pin 26) is adjusted to center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in operation. The -TEST line also contains a pull-up resistor, so adjustments can be performed simply by grounding the -TEST pin, overriding the pull-up. The -TEST pin cannot be used to disable stepping rates during operation as its function is quite different from the SAB 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a logic 1 condition. These are: ENP, -5/8, -ENMF, -WPRT, -DDEN, HLT, =TEST, and -MR.

General Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable either in FM or MFM formats. For FM, -DDEN should be placed to logic 1. For MFM formats, -DDEN should be placed to a logic 1. Sector lengths are determined at format time by the fourth byte in the ID field.

Sector Length Table*

Sector Length Field(hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* SAB 2795/97 may vary - see command summary.

The number of sectors per track as far as the SAB 279X is concerned can be from 1 to 255 sectors. The number of tracks as far as the SAB 279X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

General Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 279X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

for write operations, the SAB 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

Ready

Whenever a read or write command (Type II or III) is received the SAB 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the State of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG 43 may be tied to ENP to enable write precompensation on tracks 44-76.

Write Precompensation

When operating in double density mode (-DDEN = 0), the SAB 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the write precomp value is accomplished by forcing the -TEST line (Pin 22) to a logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while -TEST = 0.

Data Separation

The SAB 279X can operate with either an external data separator or its own internal recovery circuit. The condition of the -TEST line (Pin 22) in conjunction with -MR (Pin 19) will select internal or external mode.

To program the SAB 279X for external VCO, a -MR pulse must be applied while -TEST = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" double density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. -TEST is returned to a logic 1 for normal operation. Note: To

maintain this mode, -TEST must be held low whenever -MR is applied. For internal VCO operation, the TEST line must be high during the -MR pulse, then set to a logic 0 for the adjustment procedure.

A 50 k Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of typically 5-60 pF is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate data rate (500 kHz for 8" Double Density). The -DDEN line must be low while the -5/8 line is held high or the adjustment times above will be doubled.

VCO Operation

After adjustments have been made, the -TEST pin is returned to a logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses. Their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (PIN 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift i.e. the lock-up time. A balance must be accomplished between the two conditions to inhibit overresponsiveness to jitter and to prevent an extremely wide lock-up response leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:

Data Pattern in DR (HEX) SAB 279X Interpretation in FM (-DDEN = 1) SAB 279X Interpretation in MFM (-DDEN = 0) 00 thru F4 Write 00 thru F4 with CLK = FF Write 00 thru F4, in MFM F5 Not Allowed Write A1¹⁾ in MFM, Preset CRC F6 Not Allowed Write C2²⁾ in MFM F7 Generate 2 CRC Bytes Generate 2 CRC Bytes F8 thru FB Write F8 thru FB, CLK = C7, Preset CRC Write F8 thru FB, in MFM FC Write FC with CLK = D7 Write FC in MFM FD Write FD with CLK = FF Write FD in MFM FE Write FE, CLK = C7, Preset CRC Write FE in MFM FF Write FF with CLK = FF Write FF in MFM ¹⁾ Missing clock transition between bits 4 and 5

²⁾ Missing clock transition between bits 3 and 4

Type IV Commands

The Force Interrupt command is generally used to terminate a multiple sector Read or Write command or to ensure Type I status in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit set) the command will be terminated and the Busy status bit reset. The lower four bits of the command determine the conditional interrupt as follows:

- I0. Not-Ready to Ready Transition
- I1. Ready to Not-Ready Transition
- I2. Every Index Pulse
- I3. Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I3-I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I3-I0 are all set to zero (hex D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the Command Register will not automatically clear the interrupt. The hex D0 is the only command that will enable the immediate interrupt (hex D8) to clear on a subsequent load Command Register or read Status Register operation. Follow a hex D8 with D0 command. Wait 8 us (double density) or 16 us (Single density) before issuing a new command after issuing a Force Interrupt command (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt. Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are completed (CRC calculations, comparisons, etc.). More than one condition may be set at a time. If for example, the Ready to Not-Ready condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command would be hex DA. The OR function is performed so that either a Ready to Not-Ready or the next Index Pulse will cause an interrupt condition.

----- A -----

Formats

IBM 3740 Format-128 Bytes/Sector (8")

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00) ³⁾
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 thru 01)
1	Sector number (1 thru 1A)
1	00
1	F7 (2 CRCs written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs written)
27	FF (or 00)
247	FF (or 00)

¹⁾ Write bracketed field 26 times.

²⁾ Continue writing until SAB 279X interrupts out. Approx. 247 (598) bytes.

³⁾ Optional '00' on SAB 2795/97 only is allowed.

IBM System 34 Format - 256 Bytes/Sector (8")

Shown in the following table is the IBM double-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
80	4E
12	00
3	F6 (writes C2)
1	FC (Index Mark)
50	4E
12	00
3	F5 (writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs written)
54	4E
598	4E

Recommended - 128 Bytes/Sector (Mini-Diskette)

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 through 10)
1	00 (Sector length)
1	F7 (2 CRCs written)

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11  FF (or 00)
6   00
1   F7 (Data Address Mark)
128 Data (E5)
1   F7 (2 CRCs written)
10  FF (of 00)
349 FF (or 00)

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Non-Standard Formats Variations in the IBM formats are possible to a limited extent if the following requirements are met. 1. Sector size must be 128, 256, 512 or 1024 bytes. 2. Gap 2 cannot be varied from the recommended format. 3. 3 bytes of A1 must be used in MFM. In addition, the Index Address Mark is not required for operation by the SAB 219X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 219X operation, however, PLL lock up time, Motor speed variation, write splice area, etc., will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format should be used for highest system reliability. FM MFM Gap I 16 bytes FF 32 bytes 4E Gap II 1 1 bytes FF 22 bytes 4F 1 6 bytes 12 bytes A1 Gap III 10 bytes FF 24 bytes 4E 1 8 bytes 3 bytes A1 Gap IV 16 bytes FF 16 bytes 4E Recommended - 256 Bytes Sector (Mini-Diskette) Shown below is the recommended double-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request. Number Hex Value of Bytes Written 60 4E 1 2 3 F5! Write A1 1 FE (ID Address Mark) 1 Track Number! 1 Side Number! 1 Sector Number 11 through 101 1! Sector Length 1 FJ (2 CRCs written) 22 4E 12 3 F5! Write A1 1 FB! Data Address Mark 1256 Data! E5 1 F7 12 CRCs written 24 4E 21 4E 1 Write bracketed field 16 times. " Continue writing until SAB 219X interrupts out. Approx. 349 1181 bytes. 3' Byte counts must be exact. " Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM. Formats IBM 370 Format- 128 Bytes Sector (8-) Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request. Number Hex Value of Bytes Written 31 6 1 FC! Index Mark) 26 FF! or 1 6 1 FF! ID Address Mark) 1 Track Number 1 Side Number! 1 Sector Number! 1 through 101 1 1 1 FJ! 2 CRCs written) 1 1 FF! or 1 6 1 FB! Data Address Mark) 128 Data! E 1 FJ! 2 CRCs written) 2J FF! or 1 2QJ 21 FF! or 1 1 Write bracketed field 26 times. " Continue writing until SAB 219X interrupts out. Approx. 24J! 98) bytes. 31 optional 1 on SAB 2J3_13J only is allowed. IBM System 370 Format- 256 Bytes Sector (8-) Shown in the following table is the IBM double-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request. Number Hex Value of Bytes Written 80 4E 12 10 3 F6! writes C2) 1 FC! Index Mark 50 4E 1 2 3 F5! writes A1 1 FE! ID Address Mark 1 Track Number! 1 Side Number! 1 Sector Number! 1 through 101 1 1 FJ! 2 CRCs written) 22 4E 12 3 F5! writes A1 1 FB! Data Address Mark 56 Data (E5) 1 FJ! 2 CRCs written) 54 4E 21 QE Recommended - 128 Bytes Sector (Mini-Diskette) Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the

Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number Hex Value of Bytes Byte Written 40 FF (or 0) 11 6 WW 1 FE (ID Address Mark) 1 Track Number 1 S_IDe
Number (W or W1) 1 Sector Number (1 through 10) 1 WW (Sector length) 1 F7 (2 CRCs written) 11 FF (or 0) 6 WW 7 FB (Data
Address Mark) 128 Data (E6) 1 FJ (2 CRCs written) 10 FF (or 0) 34_I FF (or 0) 1 Non-Standard Formats Variations in the IBM formats
are possible to a limited extent if the following requirements are met. 1. Sector size must be 128, 256, 512 or 1024 bytes. 2. Gap 2
cannot be varied from the recommended format. 3. 3 bytes of A1 must be used in MFM. In addition, the Index Address Mark is not
required for operation by the SAB 219X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 219X operation, however, PLL
lock up time, Motor speed variation, write splice area, etc., will add more bytes to each gap to achieve proper operation. It is
recommended that the IBM format should be used for highest system reliability. FM MFM Gap 1 16 bytes FF 32 bytes 4E Gap 11 1
bytes FF 22 bytes 4F 1 6 bytes 12 bytes A1 Gap 11 10 bytes FF 24 bytes 4E " Q bytes 8 bytes 3 bytes A1 Gap IV 16 bytes FF 16
bytes 4E Recommended -256 Bytes Sector (Mini diskette) Shown below is the recommended double density format with 256
bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the
following values. For every byte to be written, there is one data request. Number Hex Value of Bytes Byte Written 60 4E 1' 2 3
F5 (Write A1) 1 1 FE (ID Address Mark) 1 Track Number 1 1 Side Number 1 1 Sector Number 11 through 10 1
1 Sector Length 1 FJ (2 CRCs written) 22 4E 12 3 F5 (Write A1) 1 1 FB (Data Address Mark) 256 Data 1 E5 1 1 F7 12 CRCs written 24
4E 21 4E ' Write bracketed field 16 times. " Continue writing until SAB 219X interrupts out. Approx. 349 1181 bytes. 3' Byte
counts must be exact. " Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM. ----- B ----- C -----
Absolute ____ i_u ____ i_gg'l Ambient Temperature Under Bias O to 100 °C Storage Temperature -65 to +150 °C Voltage on Any
Pin with Respect to Ground 4 IVSSJ -O 5 to -7 V Power Dissipation 2 W D.C. Characteristic TA - - O to 100 °C; VCC - 5V 5V to.
VSS - OV Symbol Parameter Limit Value Units Test Conditions Min. Typ. Max. IIL 1 ' Input Leakage Current" - 10 nA V_{IN} = V_{CC}
IIL 2 Internal Leakage Current 100 nA V_{IN} = 0V IOL Output Leakage Current - 10 VOUT = VCC V_{IH} Input High Voltage 2.0
- V_{IL} Input Low Voltage - 0.8 - V_{OH} Output High Voltage 2.4 - V_{IOH} = -I_{OL} (.IP. V_{OL} Output Low Voltage - - 0.45 IOL - 1.6
mA V_{OH} Output High PUMP 2.2 - I_{OH} 1.0 mA -V_{OL} Output Low PUMP - 0.2 IOLP - 1.0 mA I_{CC} Supply Current - 70
750 mA All outputs open C_p capacitance 31 Symbol Parameter Limit Value Units Test Conditions (max.) CIN Input Capacitance F
unmeasured p_{co} J_T output p_L capacitance 15 pF returned to GND " Stresses above those listed under..Absolute Max. I_M M
Ratings" may cause permanent damage to the device exposure to absolute maximum rating conditions for extended periods
may affect device reliability " IIL 1 3 pF I_{ESD} to normal inputs. IIL 2 to input switch Internal pull-up resistor on pins 1, 11, 19,
22, 36, 37, and 40 Also pin 2 on SAB 279112J93. 3' This parameter is periodically sampled and not 100% tested. ----- D -----
A.C. Characteristics TA 0 to 100 °C VCC - +5V 5V; VSS - OV. All timing readings at VOL = 0.8 V and V_{OH} 2.0 V.
Read Enable Timing Symbol Parameter Limit Value Units Test Conditions Min. Typ. Max. TSET Setup ADDR & CS to -RE 50
THLD Hold ADDR & CS from -RE IO - - - TRE -Rf Pulse Width 200 ns CL - 50 pF TDRR DRO Reset from -RE IO 200 ns TIRR

INTRO Reset from -RE _ 500 3000 - TDACC Data Valid from -Rf IOO 200 - CL _ 50 pF TDOH Data Hold from RE 20 - 150
 DRCl rising edge. Indicates that the data register has assembled data. DRO falling edge. Ind_icates that the data register was read.
 INTRO rising edge. Occurs at end of command. INTRO falling edge. Indicates that the status register was read. ' -CS May be
 permanently tied LOW If desired. " T Service l worst cageJ - FM - 2J. _ LIs ' Time doubles when CLK --_ 7 MHz. - MFM _ - 13. _ i. _g
 remove env.avXY: 9 11 XY: 143 32 Write Enable Timing Symbol Parameter Llrnit Values Units Tes_ Conditiong M_n_ @rvp_
 Max_ TSET Setup ADDR & CS to -WE _O THLD Hald ADDR & CS from WE IO - - TWf -WE Pulse Width 200 TD__ _ - nS _ DR
 ReSet trOm WE IOO 200 TIRR INTRCl Reset from W___E 500 3000 TDS Data Selup to WE 150 TDH Dala Hold from _W--_E 50 -
 DRCl rising edge. Ind_icates l hat the data register is empty. DRo falling edge. Indicates that the data register is loaded. INTRo risin3
 edge. Indicale the end of a command. INTRo falling edge. Indicates thall he comMand regisler is written to. I CS Mav perManenrlvtied
 Low it desired when writing c>ata into Sector, Trac_or Data Register. the user cannot read this register unt_Il at least 4Lcs in MFM
 after the rising edge_ e of WE When writ_In_ _Inlo l he Command Register status is nolualid until some 28LIS in FM174_is _In MFM
 later. TheSet_ImeS double when CLK 1 MHz. I T service l worst case; FM 23. _i.cs. MFM 1 1. _i.cs. I TiMe doub_eg when CLK 1
 MHz. ----- E ----- remove env.avXY: 9 11 XY: 141 32 remove env.avXY: 9 11 XY: 142 64 SAB 219_ Miscellaneous_ming
 Svmbl Parameter Limit Values Unit Test Condilions M_n_ @Tvp_ Max_ TCD 1 Clock Outv llowl @ 230 250 20000 nS TCD 2
 Clock Du_ lh_ghl - TSTP' Step Pulse Outpul 2 or4 - TOIR DIRC Setupto Step - 12 _ CL_ Error TM_ Mggte_ _ege_ pu_ge w._dt_ _o
 - _S TIP Index Pulse Width IO _ - RPW Read Window Pulse Width 120 700 MFM 240 - 1400 FM+1501o _ Input O-5V PreComp
 AdJ_USt IOO 300 MFM nS W_ Wr_te Data Pulge W_ldth 200 300 400 Precomp - IOOnS MFM 600 900 1200 Precomp - 300ns
 MFM VCO Free Run Voltage Controlled Oscillalor. 6.O - Ce_ = _ Adjustable bv Ext. Capacitor on Pin 26 4 o Ce_ - 3_pF Oscillator.
 Adjustable - ' - - Pump Up +2501o 5.O PU = 2.2V. Cext - 35pF p D 2_o_ 3 o MHI -po o 2v C 3_ F Ump OWn - o - , - _ , e Xt = p
 5'ID Change VCC 3.8 - 4.2 Celct = 35pF 3.5 - TA - J5'C. Cext = 35pF Adjustable External Capacitor 20 35 IOO pF VCO = 4.O MHI
 nom. RCL_ Derived Read Clock - VCO. 8. 16, 32 500 -ODEN - _ -518 = 1 250 -DDEN = _ -518 __ vCo 4 o - 2_o - kHI _ - _ MH_ --
 ' -518 =- 1 125 -DDEN = 1 -518 = _ PUI PUI-PD Time On IPulse Width) 250 MFM OON - _oo nS FM 71 _ee gtepping ra_eg on page
 _3 ----- F ----- ----- G ----- OrderingIn_ormation Component _scription Ordering Code SAB2791-02-P Floppv-Disk Controller.
 06JIXIYBI Invened Data Bus.singlesidedoperation SAB2J93_02_P Floppv_Disk Controller. 06J12_YB2 True Data
 Bus.singlesidedoperalion SAB2J9_-02_P Floppv-Disk Controller. 067120-YB3 Invened Data Bus,doublesidedoperalion SAB2J97-02-
 P Floppv-Disk Controller. _67120-Y84 True Data Bus.doublesidedoperalion