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;----- BOOT UP CPM FROM HARD DISK ON S100COMPUTERS IDR BOARD -----
;BOOT UP THE 8255/IDE Board HARD DISK/Flash Memory Card
;NOTE CODE IS ALL HERE IN CASE A 2716 IS USED

HBOOTCPM:
    POP     HL                ;CLEAN UP STACK
    LD      HL,SPEAKCPM_MSG   ;Announce on speaker
    CALL    SPEAK$

    CALL    INITILIZE_IDE_BOARD ;Initilze the 8255 and drive (again just in case)

    LD      D,11100000B       ;Data for IDE SDH reg (512bytes, LBA mode,single drive)
    LD      E,REGshd          ;00001110, (0EH) CS0,A2,A1,
    CALL    IDEwr8D           ;Write byte to select the MASTER device

    LD      B,0FFH            ;Delay time

WaitInit:
    LD      E,REGstatus       ;Get status after initilization
    CALL    IDErd8D           ;Check Status (info in [D])
    BIT     7,D
    JR      Z,SECREAD         ;Zero, so all is OK to write to drive
                                ;Delay to allow drive to get up to speed

    PUSH    BC
    LD      BC,0FFFFH

DXLAY2: LD      D,2            ;May need to adjust delay time to allow cold drive to
DXLAY1: DEC     D              ;to speed
    JR      NZ,DXLAY1
    DEC     BC
    LD      A,C
    OR      B
    JR      NZ,DXLAY2
    POP     BC
    DJNZ   WaitInit

IDError:
    LD      HL,DRIVE_NR_ERR    ;Drive not ready
    JP      ABORT_ERR_MSG

SECREAD:
                                ;Note CPMLDR will ALWAYS be on TRK 0,SEC 1,Head 0
                                ;FLAG PROGRESS VISUALLY FOR DIAGNOSTIC
    LD      A,11111111B
    OUT     (DIAG_LEDS),A

    CALL    IDEwaitnotbusy     ;Make sure drive is ready
    JR      C,IDError          ;NC if ready

    LD      D,1                ;Load track 0,sec 1, head 0
    LD      E,REGsector        ;Send info to drive
    CALL    IDEwr8D

    LD      D,0                ;Send Low TRK#
    LD      E,REGcyLSB
    CALL    IDEwr8D

    LD      D,0                ;Send High TRK#
    LD      E,REGcyMSB
    CALL    IDEwr8D

    LD      D,SEC_COUNT        ;Count of CPM sectors we wish to read
    LD      E,REGcnt
    CALL    IDEwr8D

    LD      D,CMDread          ;Send read CMD
    LD      E,REGCMD
    CALL    IDEwr8D           ;Send sec read CMD to drive.
    CALL    IDEwdrq           ;Wait until it's got the data

    LD      HL,CPM_ADDRESS     ;DMA address where the CPMLDR resides in RAM
    LD      B,0                ;256X2 bytes
    LD      C,SEC_COUNT        ;Count of sectors X 512

MoreRD16:
    LD      A,REGdata          ;REG regsiter address
    OUT     (IDECport),A

    OR      IDErcline         ;08H+40H, Pulse RD line
    OUT     (IDECport),A

    IN      A,(IDEAport)       ;read the LOWER byte
    LD      HL,A
    INC     HL

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IN      A, (IDEBport)          ;read the UPPER byte
LD      (HL),A
INC     HL

LD      A,REGdata             ;Deassert RD line
OUT     (IDECport),A
DJNZ   MoreRD16
DEC     C
JR      NZ,MoreRD16

LD      E,REGstatus          ;Check the R/W status when done
CALL   IDErd8D
BIT    0,D
JR      NZ,IDEerr1           ;Z if no errors
LD      HL,STARTCPM
LD      A,(HL)
CP     31H                   ;EXPECT TO HAVE 31H @80H IE. LD SP,80H
JP     Z,STARTCPM           ;AS THE FIRST INSTRUCTION. IF OK JP to 100H in RAM
JP     ERR_LD1              ;Boot Sector Data incorrect

IDEerr1:
LD      HL,IDE_RW_ERROR      ;Drive R/W Error
JP     ABORT_ERR_MSG

;      ----- SUPPORT ROUTINES -----

INITILIZE_IDE_BOARD:
LD      A,RDcfg8255          ;Drive Select in [A]. Note leaves selected drive as [A]
OUT     (IDECtrl),A         ;Config 8255 chip (10010010B), read mode on return
                                ;Config 8255 chip, READ mode

                                ;Hard reset the disk drive
                                ;For some reason some CF cards need to the RESET line
                                ;pulsed very carefully. You may need to play around
                                ;with the pulse length. Symptoms are: incorrect data comming
LD      A,IDEReset          ;back from a sector read (often due to the wrong sector being read)
OUT     (IDECport),A       ;I have a (negative)pulse of 2.7uSec. (10Mz Z80, two IO wait states).
                                ;Which seem to work for the 5 different CF cards I have

LD      B,020H
ResetDelay:
DEC     B
JP     NZ,ResetDelay        ;Delay (reset pulse width)

CALL   DELAY_32             ;Need to stretch pulse!
XOR    A
OUT     (IDECport),A       ;No IDE control lines asserted (just bit 7 of port C)

IDEwaitnotbusy:
LD      B,0FFH              ;Drive READY if 01000000
LD      C,080H              ;Delay, must be above 80H for 4MHz Z80. Leave longer for slower drives

MoreWait:
LD      E,REGstatus          ;Wait for RDY bit to be set
CALL   IDErd8D
LD      A,D
AND    11000000B
XOR    01000000B
JR      Z,DoneNotbusy
DJNZ   MoreWait
DEC     C
JR      NZ,MoreWait
SCF                                  ;Set carry to indicate an error
RET

DoneNotBusy:
OR     A                      ;Clear carry it indicate no error
RET

                                ;Wait for the drive to be ready to transfer data.
                                ;Returns the drive's status in Acc

IDEwdrq:
LD      B,0FFH
LD      C,0FFH              ;Delay, must be above 80H for 4MHz Z80. Leave longer for slower drives

MoreDRQ:
LD      E,REGstatus          ;wait for DRQ bit to be set
CALL   IDErd8D
LD      A,D
AND    10001000B
CP     00001000B
JR      Z,DoneDRQ
DJNZ   MoreDRQ
DEC     C
JR      NZ,MoreDRQ

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        SCF                ;Set carry to indicate error
        RET
DoneDRQ:
        OR      A          ;Clear carry
        RET
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; Low Level 8 bit R/W to the drive controller.  These are the routines that talk
; directly to the drive controller registers, via the 8255 chip.
; Note the 16 bit I/O to the drive (which is only for SEC Read here) is done directly
; in the routine MoreRD16 for speed reasons.

IDErD8D:
        LD      A,E        ;READ 8 bits from IDE register in [E], return info in [D]
        OUT    (IDECport),A ;drive address onto control lines

        OR      IDErdline  ;RD pulse pin (40H)
        OUT    (IDECport),A ;assert read pin

        IN     A,(IDEAport)
        LD     D,A        ;return with data in [D]

        LD     A,E        ;<---Ken Robbins suggestion
        OUT    (IDECport),A ;Deassert RD pin

        XOR    A
        OUT    (IDECport),A ;Zero all port C lines
        RET

IDEwr8D:
        LD     A,WRCfg8255 ;WRITE Data in [D] to IDE register in [E]
        OUT    (IDECtrl),A ;Set 8255 to write mode

        LD     A,D        ;Get data put it in 8255 A port
        OUT    (IDEAport),A

        LD     A,E        ;select IDE register
        OUT    (IDECport),A

        OR     IDEwrline  ;lower WR line
        OUT    (IDECport),A

        LD     A,E        ;<-- Kens Robbins suggestion, raise WR line
        OUT    (IDECport),A

        XOR    A
        OUT    (IDECport),A ;Deselect all lines including WR line

        LD     A,RDCfg8255 ;Config 8255 chip, read mode on return
        OUT    (IDECtrl),A
        RET

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