APPENDIX A
DC CHARACTERISTICS

Absolute Maximum Rating

Storage Temperature Range:	-65 C to +150 C
Active Temperature Range:	-55 C to +125 C
Supply Voltage:	+7.0V
Input or Output Voltage Applied:	Vss -0.3V Vcc +0.3V

Electrical Characteristics

Specified Temperature Range	0 C to +70 C
Specified Voltage Range	+4.75V to +5.25V
Test Conditions	Temperature = +70 C Vss = 0V Vcc = +4.75V (except as noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IH}	High level MOS input	70% V_{cc}		V	
V_{IL}	Low level MOS input		30% V_{cc}	V	
V_{IHT}	High level TTL input	2.2		V	
V_{ILT}	Low level TTL input		0.8	V	
I_I	Input leakage current except TEST inputs (note 1)	-10.0	10.0	uA	$0V \leq V_I \leq V_{cc}$
I_{ILL}	Input current TEST inputs (note 1)	0.1	5.0	mA	$V_I = 0V$
I_{OH}	Output current at high level	-2.0		mA	$V_O = V_{cc} - 0.4V$
I_{OL}	Output current at low level	2.0		mA	$V_O = 0.4V$

Symbol	Parameter	Min.	Max.	Units	Test Condition
I_{OHT}	Output current at high TTL level	-2.0		mA	V_O = 2.4V
I_{OSH}	High level sustainer current (note 1)	-0.2	-0.6	mA	$V_O = V_{CC} - 1.0V$
I_{OSL}	Low level sustainer current (note 1)	0.2	0.6	mA	V_O = 1.0V
I_{OZ}	Output leakage current (notes 1,2)	-10.0	10.0	uA	$0V \leq V_O \leq V_{CC}$
I_{CCSB}	Static power supply current (notes 1,3)		30	mA	
C_{IN}	Input capacitance (note 4)		7	pF	
C_{IO}	Input/output capacitance (note 4)		15	pF	
C_{OUT}	Output capacitance (note 4)		15	pF	
C_{MAX}	DCJ11 capacitance plus external capacitance		50	pF	

NOTES

1. Tested at Vcc = 5.25V.
2. Only applies in the high impedance condition.
3. With TEST1 and TEST2 asserted, all outputs open circuit, and all other inputs equal to Vcc.
4. Sampled and guaranteed, but not tested. Does not apply to TEST1 or TEST2.

SIGNAL SUMMARY

TYPE	NAME	APPLICABLE DC TEST
TTL INPUT	IRQ<3:0>, HALT, PWRF, EVENT, PARITY, DV, MISS, CONT, DMR, INIT, FPE	V_{IHT} , V_{ILT} , I_I
TTL OUTPUT	DAL<21:16>, AIO<3:0>, ALE, BUFCTL, SCTL, STRB, BS<1:0>, MAP, PRDC	I_{OL} , I_{OHT} , I_{OZ}
MOS INPUT	TEST1, TEST2	V_{IH} , V_{IL} , I_{ILL}
MOS OUTPUT	CLK, CLK2	I_{OH} , I_{OL} , I_{OZ}
TTL I/O	ABORT*	V_{ILT} , I_{OL} , I_{OHT} , I_{OZ} , I_{OSH}
TTL I/O	DAL<15:00>	V_{IHT} , V_{ILT} , I_{OL} , I_{OHT} , I_{OZ}
Power	Vcc	I_{CCSB}

* ABORT must be driven with an open collector driver because the DCJ11 has a pull-up device that supplies I_{OSH} .

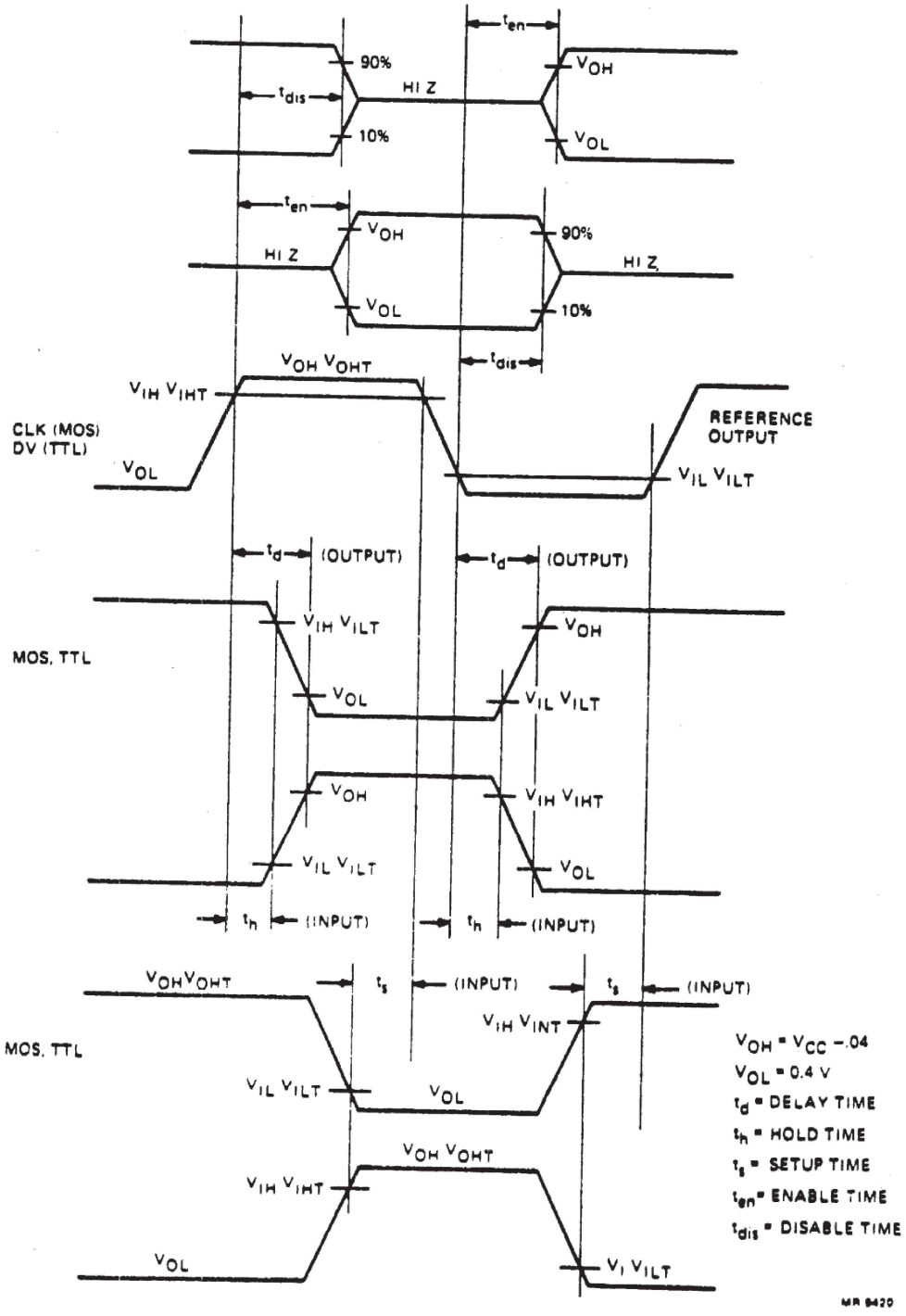


Figure A-1 Voltage Waveforms

Test Conditions:

Temperature = +70 C
Vss = 0V
Vcc = +4.75V (except as noted)
CMAX = 50 pF

Timing Requirements

Symbol	Parameter	Min	Max	Units
t_{INITW}	$\overline{INIT}$ pulse width	10		clock periods
t_{SCTLLH}	Initialization interval	225		ns
t_{DS}	DAL<15:00> setup, with respect to T3	35		ns
t_{DH}	DAL<15:00> hold, with respect to T3	20		ns
t_{DVDS}	DAL<15:00> setup, with respect to DV	35		ns
t_{DVDH}	DAL<15:00> hold, with respect to DV	35		ns
t_{DVW}	DV Pulse width	35		ns
t_{DVF}	DV Fall time		15	ns
t DVH	DV deassertion with respect to T6.	0		ns
t DVS	DV deassertion with respect to T4.	0		ns
t_{HMS}	$\overline{MISS}$ setup	30		ns
t_{HMH}	$\overline{MISS}$ hold	10		ns
t_{SVCS}	IRQ<3:0>, $\overline{HALT}$, $\overline{PWRF}$, $\overline{FPE}$, $\overline{EVENT}$ setup (see note)	20		ns

Symbol	Parameter	Min	Max	Units
t_{SVCH}	IRQ<3:0>, HALT, PWRF, FPE, EVENT hold (see note)	20		ns
t_{PARS}	PARITY setup (see note)	20		ns
t_{PARH}	PARITY hold (see note)	20		ns
t_{ABS}	ABORT drive	30		ns
t_{ABD}	ABORT delay	0		ns
t_{ABW}	ABORT width	40 + t_{CLKH}		ns
t_{CNTS}	CONT setup (see note)	30		ns
t_{CNTH}	CONT hold (see note)	20		ns
t_{DMRS}	DMR setup (see note)	30		ns
t_{DMRH}	DMR hold (see note)	20		ns

Note:
Setup and hold requirements are only to guarantee recognition at next sample point.

Timing Responses

Symbol	Parameter	Min	Max	Units	Figure References
t_{CYCLE}	CLK cycle time	67		ns	B-1, B-4
t_{CLKH}	CLK high width	28		ns	B-1, B-4
t_{CLKL}	CLK low width	28		ns	B-1, B-4
t_{R}	CLK rise time		7	ns	B-1, B-4
t_{F}	CLK fall time		7	ns	B-1, B-4
t_{PCYC}	CLK2 cycle time	67		ns	B-1, B-3
t_{PCLKH}	CLK2 high width	28		ns	B-1, B-3

Symbol	Parameter	Min	Max	Units	Figure References
t_{PCLKL}	CLK2 low width	28		ns	B-1, B-3
t_{PR}	CLK2 rise time		7	ns	B-1, B-3
t_{PF}	CLK2 fall time		7	ns	B-1, B-3
t_{PCLKD}	CLK2 valid delay		tbs	ns	B-1, B-3
t_{MAPD}	MAP delay		45	ns	B-1, B-3
t_{SD}	Strobe active delay	0		ns	B-3
t_{SID}	Strobe inactive delay	0		ns	B-3
t_{DIS}	DAL output disable		35	ns	B-2
t_{DALD}	DAL valid delay		65	ns	B-3
t_{DALH}	DAL valid hold	0		ns	B-3
t_{PD}	PRDC valid delay		50	ns	B-3
t_{PID}	PRDC invalid delay		50	ns	B-3
t_{AIOD}	AIO<3:0> delay		75	ns	B-3

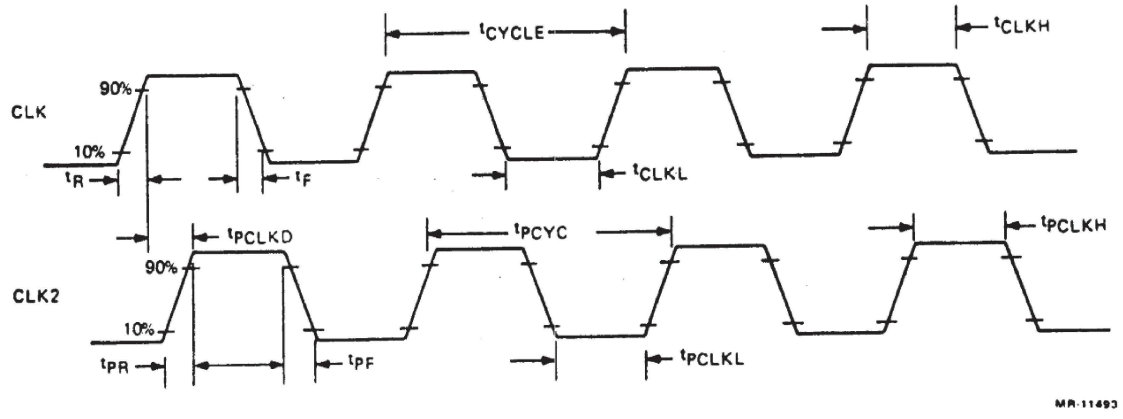


Figure B-1 Clock Timing

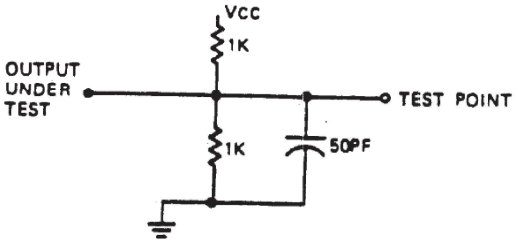


Figure B-2
Three State
Disable Test Circuit

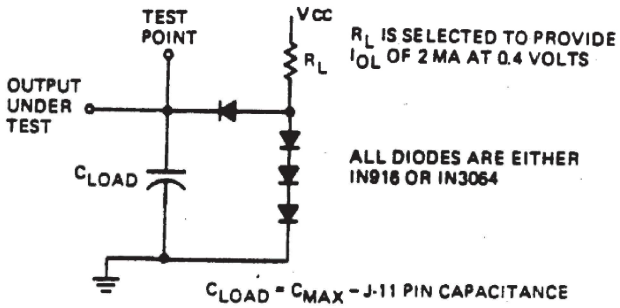


Figure B-3
TTL Output Test Circuit

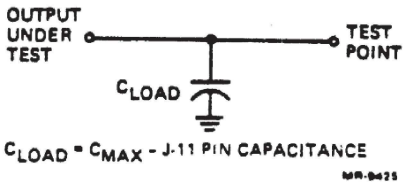


Figure B-4
MOS Output Test Circuit

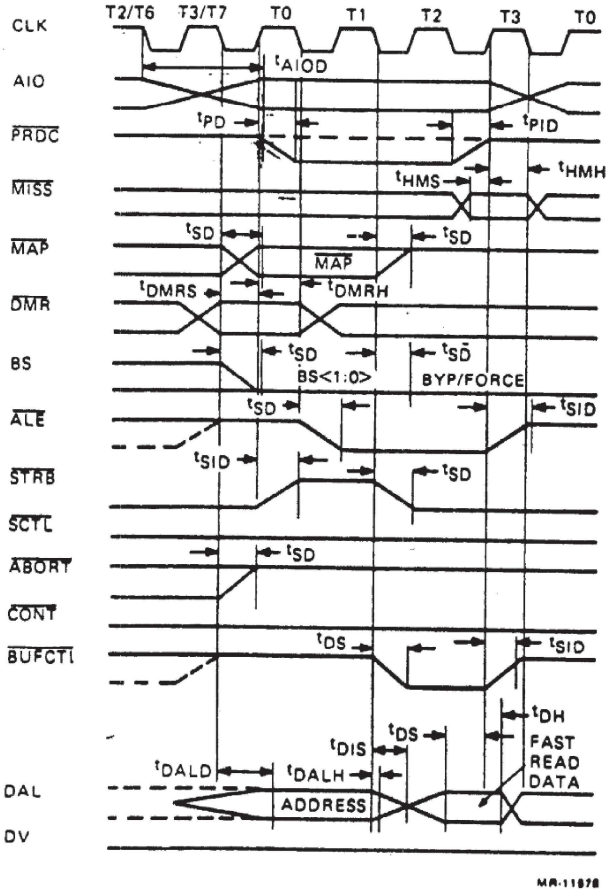


Figure B-5 Non-Stretched Bus Read Timing

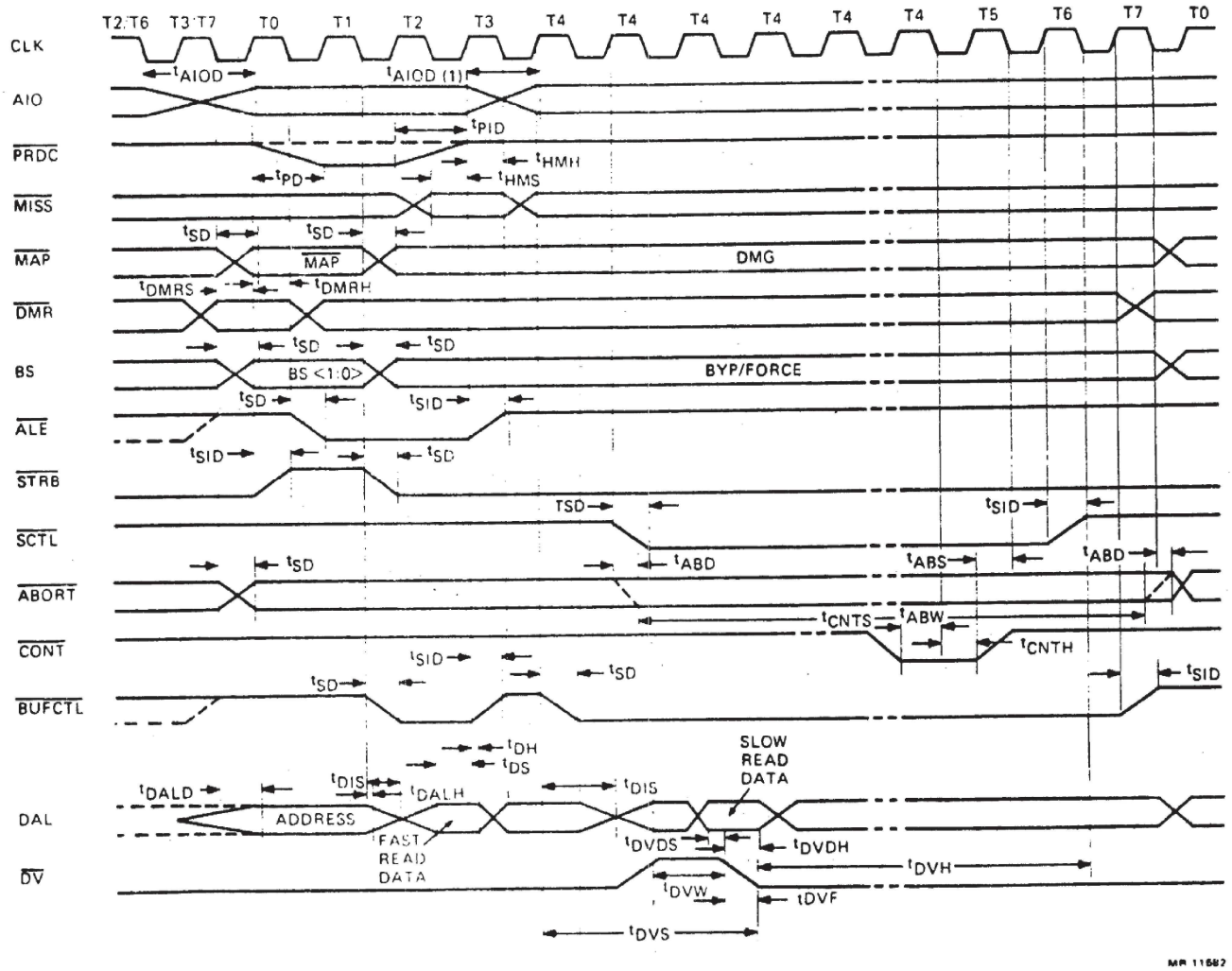


Figure B-6 Stretched Bus Read Timing

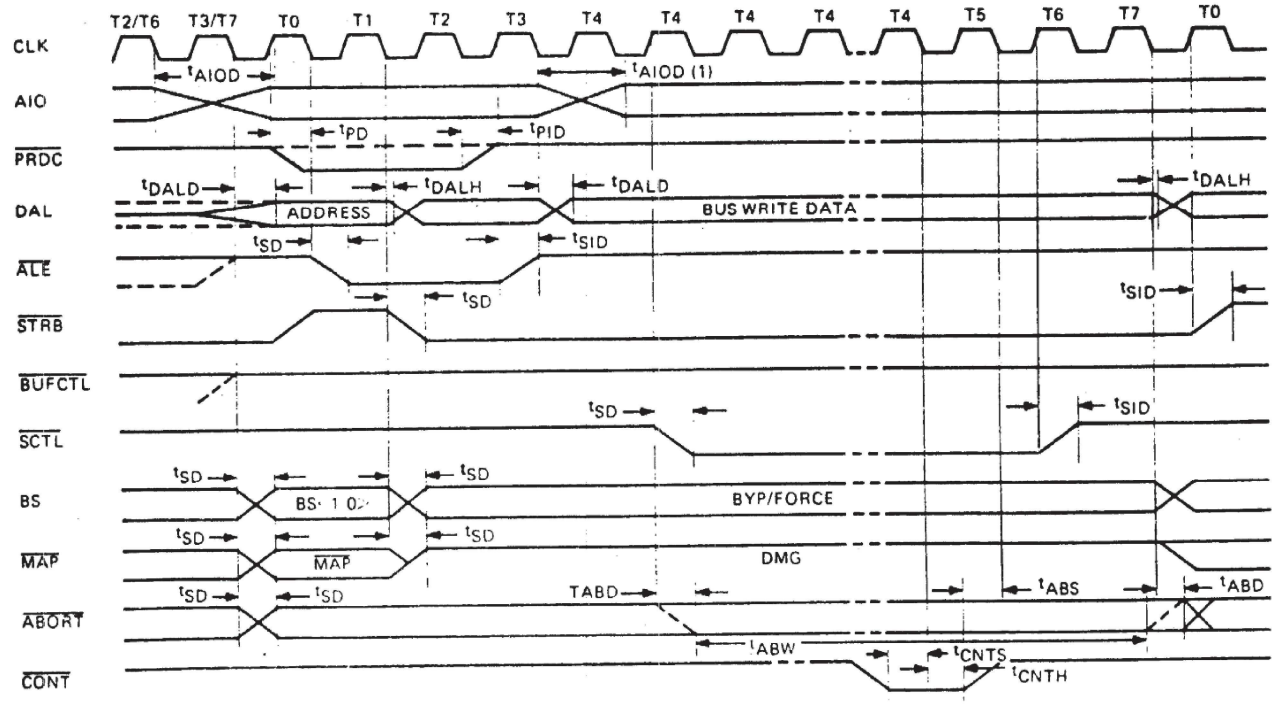


Figure B-7 Bus Write Timing

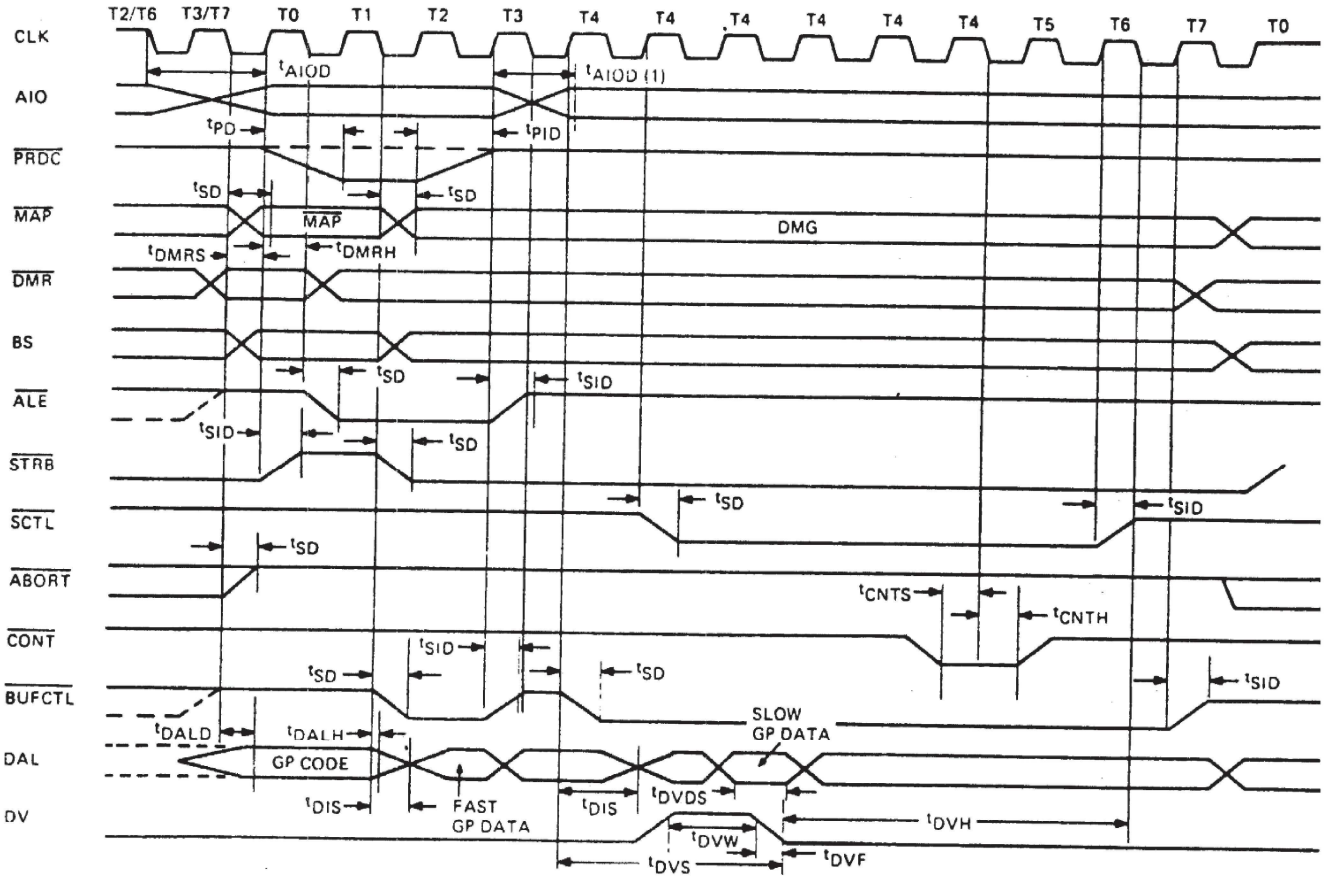


Figure B-8 General-Purpose Read Timing

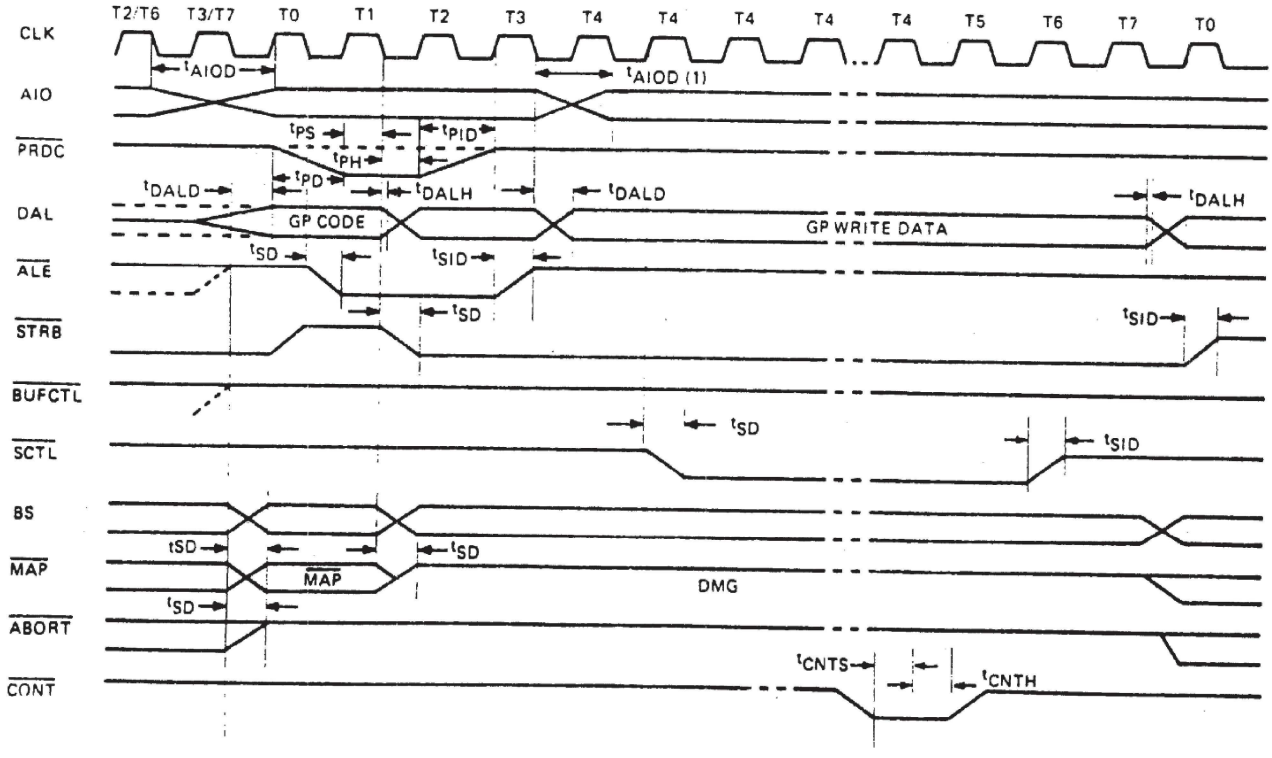


Figure B-9 General-Purpose Write Timing