

## 8.1 INTRODUCTION

This chapter covers topics related to the interfacing of external logic to the DCJ11.

## 8.2 GENERAL-PURPOSE (GP) CODES

An important means of communicating with external logic is through the use of GP Reads and Writes (see Chapter 3 - Bus Cycles). GP Reads and Writes are associated with codes that specify the function performed during the GP Read or Write cycle. External logic interprets these codes to implement system functions. Table 8-1 summarizes the GP codes.

Table 8-1 GP Codes and Functions

GP Code (octal)	GP Read or Write	Function
000	Read	Reads the power-up mode, HALT option, FPA option, POK, and boot address.
001	Read	Reads FPA data (if FPA exists)
002	Read	Reads the power-up mode, HALT option, FPA option, POK, and boot address, and (if an FPA exists) clears the FPA's FPS.
003	Read	Acknowledges FPE and reads the FEC (floating exception code) register
003	Write	Writes FPA 16-bit data (if FPA exists)
014	Write	Asserts bus reset signal
034	Write	Signals exit from console ODT
040	Write	Reserved for future use
100	Write	Acknowledges EVENT
140	Write	Acknowledges power fail
214	Write	Negates bus reset signal
220	Write	Microdiagnostic test 1 passed
224	Write	Microdiagnostic test 2 passed
230	Write	Microdiagnostic test 3 passed
234	Write	Signals entry into console ODT

Specific external logic designs may need to interpret only a subset of the GP codes. For example, a minimal system with no FPA and no need for POK or a bus reset signal would only have to identify a GP code associated with the reading of power-up configuration data during the DCJ11's initialization sequence. As shown in the flowchart in Paragraph 8.3.2, this is GP code 002.

### 8.3 POWER-UP AND INITIALIZATION

The DCJ11 performs a specific sequence of events at power-up or when it is initialized. These initialization microroutines are described in this paragraph. Also, during power-up the DCJ11 reads the contents of a configuration register to determine its initial mode of operation. This configuration register is also described. A typical power-up circuit is also provided.

**8.3.1 Initialization Timing -** Initialization timing is shown in Figure 8-1. When external logic asserts INIT for a minimum of 25 clock periods, the DCJ11 is forced into a power-up initialization sequence. As shown in Figure 8-1, the DCJ11 asserts SCTL shortly after the assertion of INIT. SCTL is deasserted approximately five clock periods after INIT is deasserted.

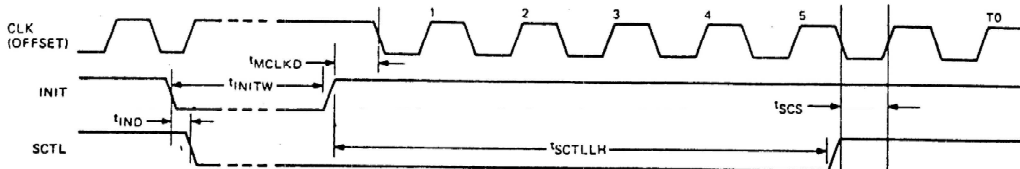
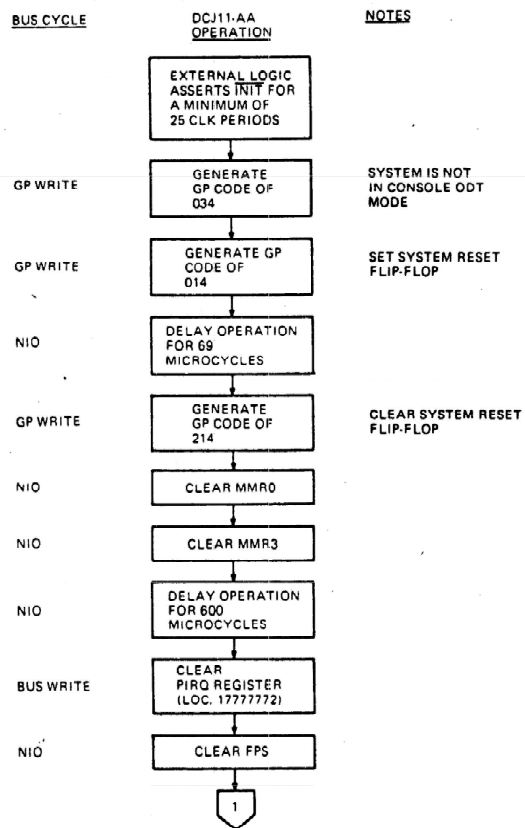


Figure 8-1 Initialization

**8.3.2 Initialization Microroutine -** The microroutine that is executed when the DCJ11 is powered up or initialized is shown in Figure 8-2. Note that GP codes that indicate some event (such as the passing of a microdiagnostic test) can be used by external logic to light LEDs for a visual indication of the event.



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Figure 8-2 Initialization Sequence

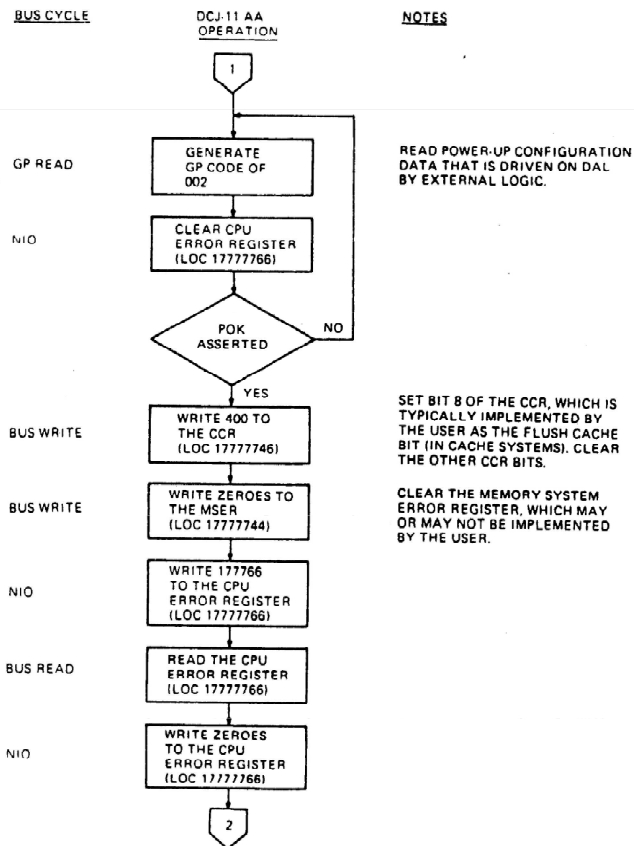
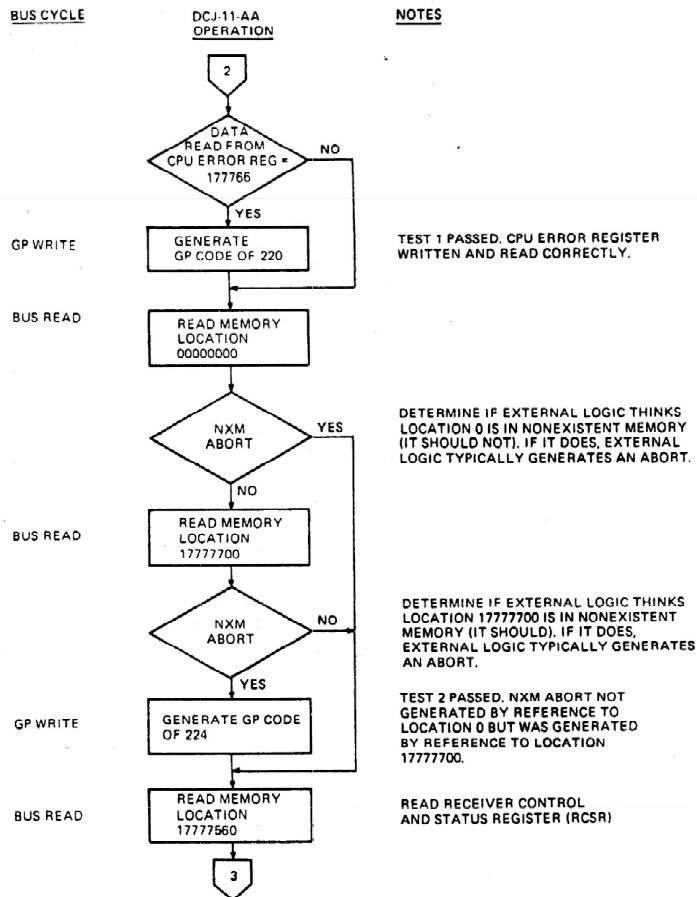


Figure 8-2 Initialization Sequence (Continued)





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Figure 8-2 Initialization Sequence (Continued)

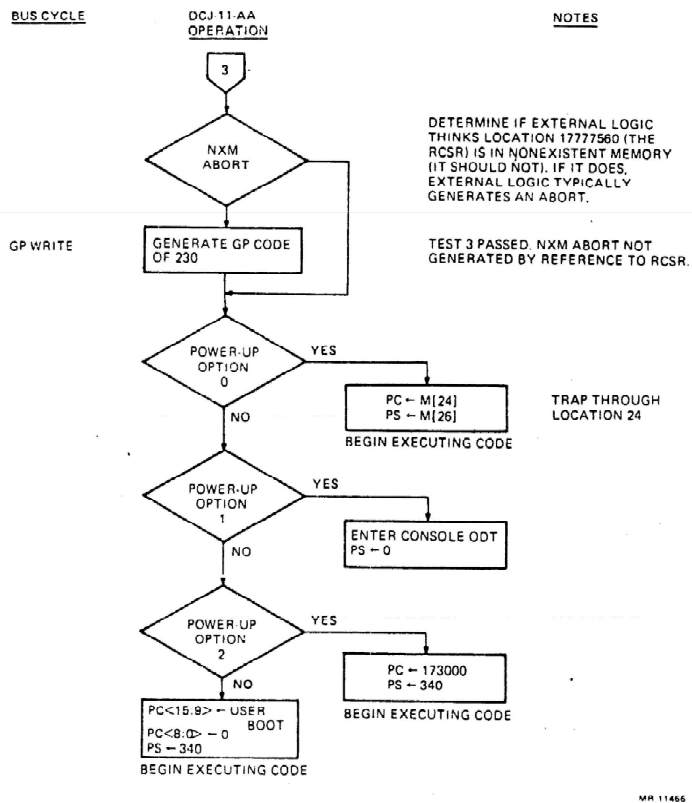


Figure 8-2 Initialization Sequence (Continued)

**8.3.3 Power-Up Configuration** - The power-up configuration is specified by setting bits in an external register which is read (via the DAL) during the DCJ11's initialization sequence. It specifies various user-defined initial conditions. The register is shown in Figure 8-3.

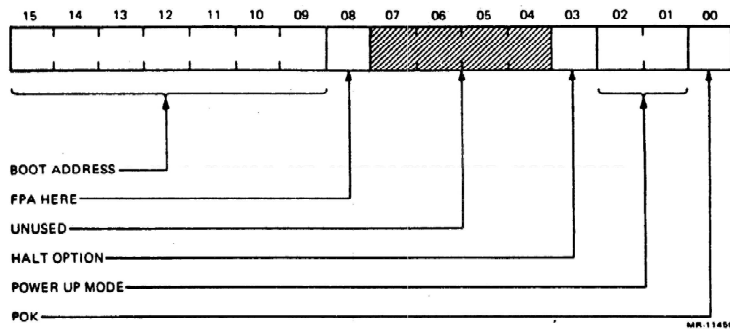


Figure 8-3 Power-Up Configuraton Register

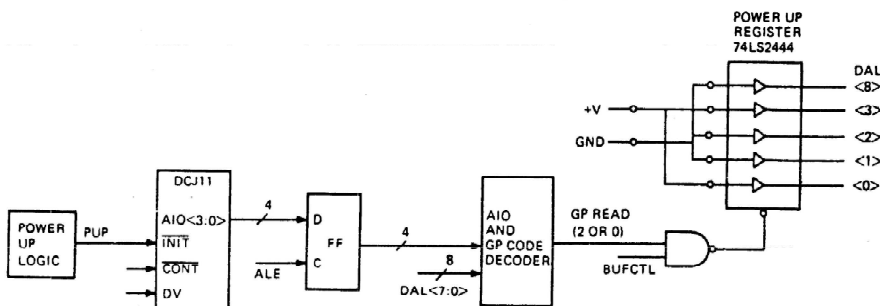
Bit(s)	Name	Description																		
<15:9>	Boot Address	Contains the most significant seven bits (bits <15:9>) of a user-defined boot address used in power-up mode 3. The lower bits of the boot address (bits <8:0>) are zeroes.																		
8	FPA Here	Indicates the presence of an optional floating-point accelerator (FPA) when set. When cleared, the FPA is not present.																		
<7:4>	Unused	These bits are not interpreted by the DCJ11.																		
3	Halt Option	Indicates how a HALT instruction will execute in kernel mode. If set, the DCJ11 traps through location 4 and sets bit 7 of the CPU error register when HALT is executed. If cleared, the DCJ11 enters console ODT when HALT is executed.																		
<2:1>	Power-Up Mode	Indicates one of four power-up mode options.																		
<table> <tr> <th colspan="2">Bits</th><th></th></tr> <tr> <td>2</td><td>1</td><td>Mode</td></tr> <tr> <td>0</td><td>0</td><td>Trap through location 24</td></tr> <tr> <td>0</td><td>1</td><td>Enter console ODT</td></tr> <tr> <td>1</td><td>0</td><td>Power-up to 17773000</td></tr> <tr> <td>1</td><td>1</td><td>Power-up to the user-defined address specified by bits &lt;15:9&gt;</td></tr> </table>			Bits			2	1	Mode	0	0	Trap through location 24	0	1	Enter console ODT	1	0	Power-up to 17773000	1	1	Power-up to the user-defined address specified by bits <15:9>
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2	1	Mode																		
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1	0	Power-up to 17773000																		
1	1	Power-up to the user-defined address specified by bits <15:9>																		
0	POK	Indicates whether the power supply																		

is operating within its normal range.  
Set when power is at an acceptable  
value.

**8.3.4 Power-Up Circuit** - A circuit such as that shown in Figure 8-4 can be used to power-up the DCJ11.

INIT is provided to the DCJ11 by power-up logic and the AIO code is latched by the assertion of ALE. The decoder indicates whether a GP Read of 000 or 002 is being executed.

In this simple application, only DAL<8,3:0> are affected by the power-up configuration register. The register is configured to indicate that no FPA is present, power-up mode 0 (trap through location 24) is selected, and power is always OK. The DAL is driven with configuration data when BUFCTL is asserted and a GP Read with a code of 000 or 002 occurs.

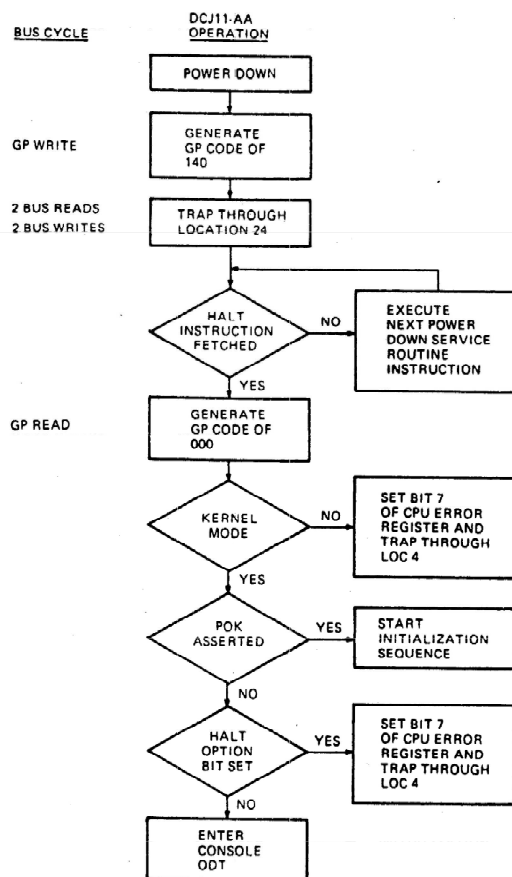


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Figure 8-4 Power-Up Circuit

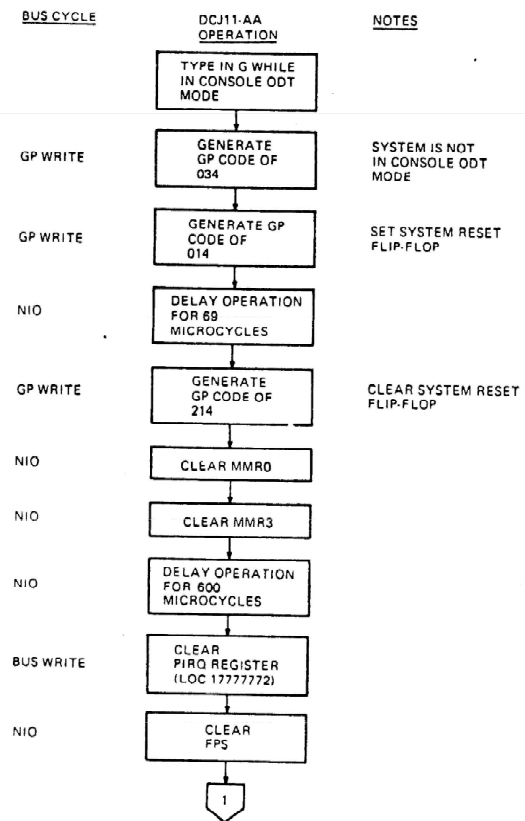
#### 8.4 OTHER MICROROUTINES

Figures 8-5 and 8-6 illustrate two other microroutines whose operation can be monitored by external logic: the power-down microroutine and the console ODT response to entering the "go" command.



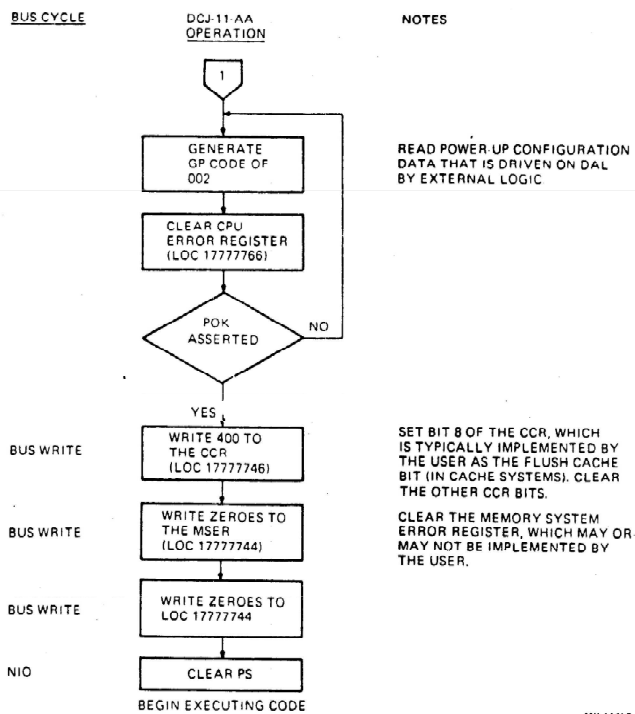
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Figure 8-5 Power-Down Sequence



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Figure 8-6 Console Start Sequence



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Figure 8-6 Console Start Sequence (Continued)