REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Sep.06.2012

FEATURES

- Fast access time : 55ns
- Low power consumption:
  Operating current : 45mA (TYP.)
  Standby current : 10μA (TYP.) SL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
  - (i) BYTE# fixed to V_{CC}
    LB# controlled DQ0 ~ DQ7
    UB# controlled DQ8 ~ DQ15
  - (ii) BYTE# fixed to V_{SS}
    DQ15 used as address pin, while LB#, UB# and DQ8~DQ14 pins not used
- Data retention voltage : 1.2V (MIN.)
- **Green package available**
- Package : 48-pin 12mm x 20mm TSOP-I

GENERAL DESCRIPTION

The AS6C3216 is a 33,554,432-bit low power CMOS static random access memory organized as 2,097,152 words by 16 bits or 4,194,304 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C3216 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C3216 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{cc},TYP.)
AS6C3216(I)	-40 ~ 85℃	2.7 ~ 3.6V	55ns	10μA(SL)	45mA

FUNCTIONAL BLOCK DIAGRAM
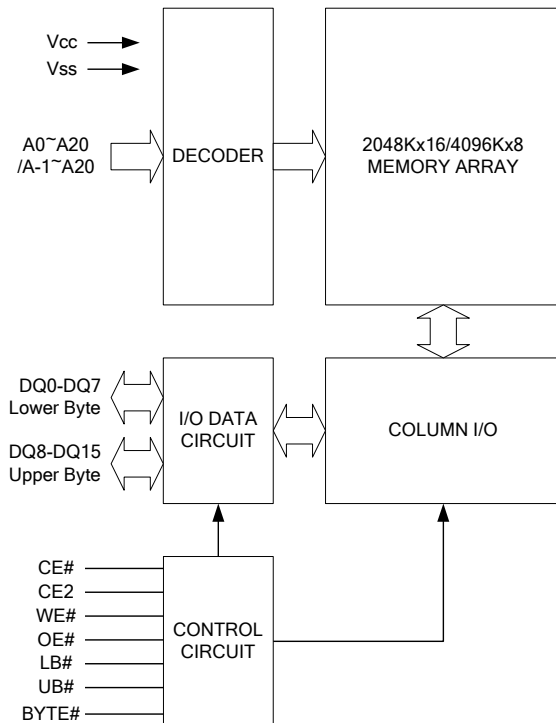
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A20	Address Inputs(word mode)
A-1 – A20	Address Inputs(byte mode)
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
BYTE#	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground

AS6C3216

32M Bits (2Mx16 / 4Mx8 Switchable) LOW POWER CMOS SRAM

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	A15		48	A16
2	A14		47	BYTE#
3	A13		46	Vss
4	A12		45	DQ15/A-1
5	A11		44	DQ7
6	A10		43	DQ14
7	A9		42	DQ6
8	A8		41	DQ13
9	A19		40	DQ5
10	A20		39	DQ12
11	WE#		38	DQ4
12	CE2		37	Vcc
13	NC		36	DQ11
14	UB#		35	DQ3
15	LB#		34	DQ10
16	A18		33	DQ2
17	A17		32	DQ9
18	A7		31	DQ1
19	A6		30	DQ8
20	A5		29	DQ0
21	A4		28	OE#
22	A3		27	Vss
23	A2		26	CE#
24	A1		25	A0

TSOP-I
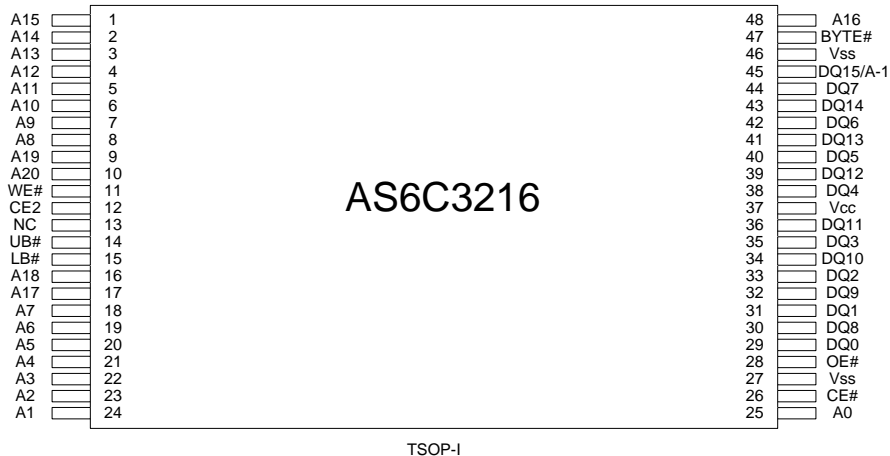
ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V_{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T_A	-40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	BYTE#	OE#	WE#	LB#	UB#	I/O OPERATION			SUPPLY CURRENT
								DQ0-DQ7	DQ8-DQ14	DQ15	
Standby	H	X	X	X	X	X	X	High – Z	High – Z	High – Z	I_{SB}, I_{SB1}
	X	L	X	X	X	X	X	High – Z	High – Z	High – Z	
	X	X	H	X	X	H	H	High – Z	High – Z	High – Z	
Output Disable	L	H	H	H	H	L	X	High – Z	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	H	H	X	L	High – Z	High – Z	High – Z	
	L	H	L	H	H	X	X	High – Z	High – Z	High – Z	
Read	L	H	H	L	H	L	H	D_{OUT}	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	L	H	H	L	High – Z	D_{OUT}	D_{OUT}	
	L	H	H	L	H	L	L	D_{OUT}	D_{OUT}	D_{OUT}	
Write	L	H	H	X	L	L	H	D_{IN}	High – Z	High – Z	I_{CC}, I_{CC1}
	L	H	H	X	L	H	L	High – Z	D_{IN}	D_{IN}	
	L	H	H	X	L	L	L	D_{IN}	D_{IN}	D_{IN}	
Byte# Read	L	H	L	L	H	X	X	Dout	High – Z	A-1	I_{CC}, I_{CC1}
Byte # Write	L	H	L	X	L	X	X	Din	High – Z	A-1	I_{CC}, I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. [4]	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH} [1]			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} [2]			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$ Output Disabled		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.2	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL} and CE2 = V_{IH} $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 55	-	45	80	mA
	I_{CC1}	Cycle time = 1μs CE#$\leqq$0.2V and CE2$\geqq V_{CC}$-0.2V $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC}-0.2V		-	10	20	mA
Standby Power Supply Current	I_{SB}	CE# = V_{IH} or CE2 = V_{IL} Other pins at V_{IL} or V_{IH}		-	0.3	2	mA
	I_{SB1}	CE# $\geqq V_{CC}$-0.2V or CE2$\leqq$0.2V Other pins at 0.2V or V_{CC}-0.2V	-SLI	-	10	120	μA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE $(T_A = 25℃, f = 1.0MHz)$

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C3216-55		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	ns
Address Access Time	t_{AA}	-	55	ns
Chip Enable Access Time	t_{ACE}	-	55	ns
Output Enable Access Time	t_{OE}	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	20	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	20	ns
Output Hold from Address Change	t_{OH}	10	-	ns
LB#, UB# Access Time	t_{BA}	-	55	ns
LB#, UB# to High-Z Output	t_{BHZ}*	-	25	ns
LB#, UB# to Low-Z Output	t_{BLZ}*	10	-	ns

(2) WRITE CYCLE

| PARAMETER	SYM.	AS6C3216-55		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	ns
Address Valid to End of Write	t_{AW}	50	-	ns
Chip Enable to End of Write	t_{CW}	50	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	45	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	20	ns
LB#, UB# Valid to End of Write	t_{BW}	45	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)
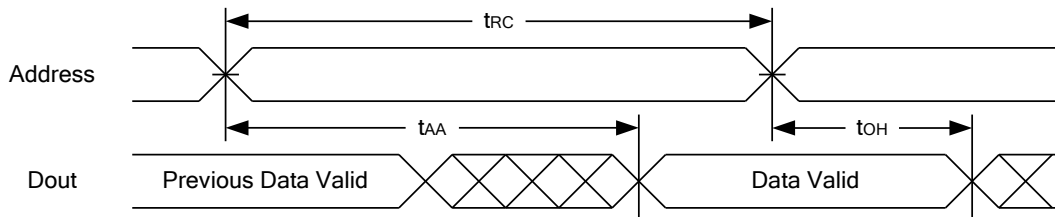
**READ CYCLE 2** (CE# and CE2 and OE# Controlled) (1,3,4,5)
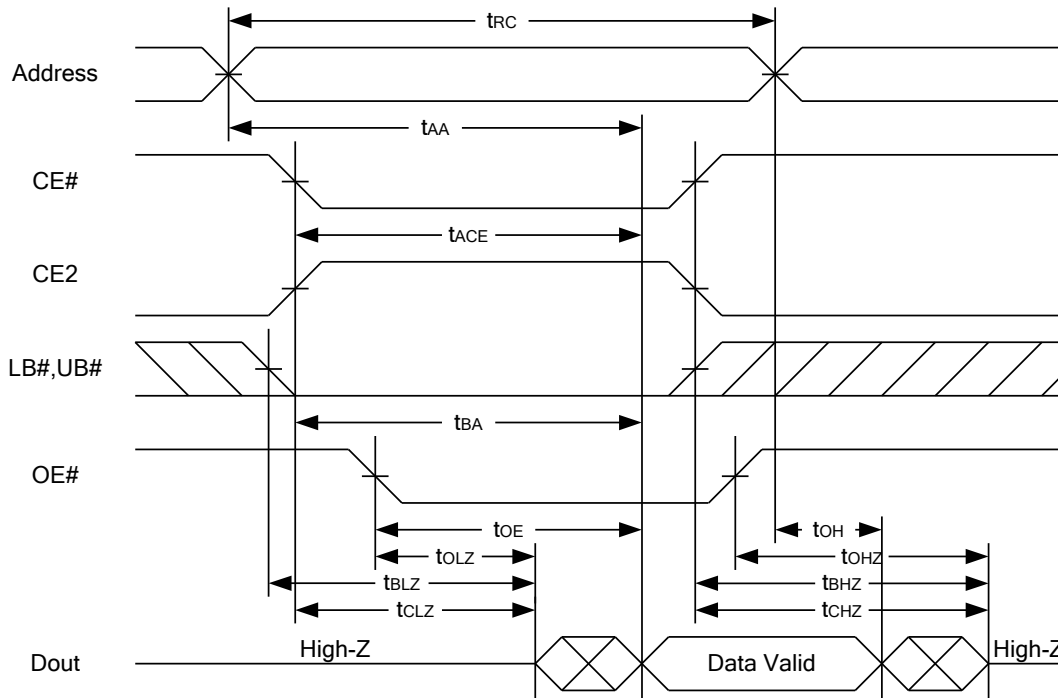
Notes :

1.WE#is high for read cycle.

2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.

3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.

4.t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)
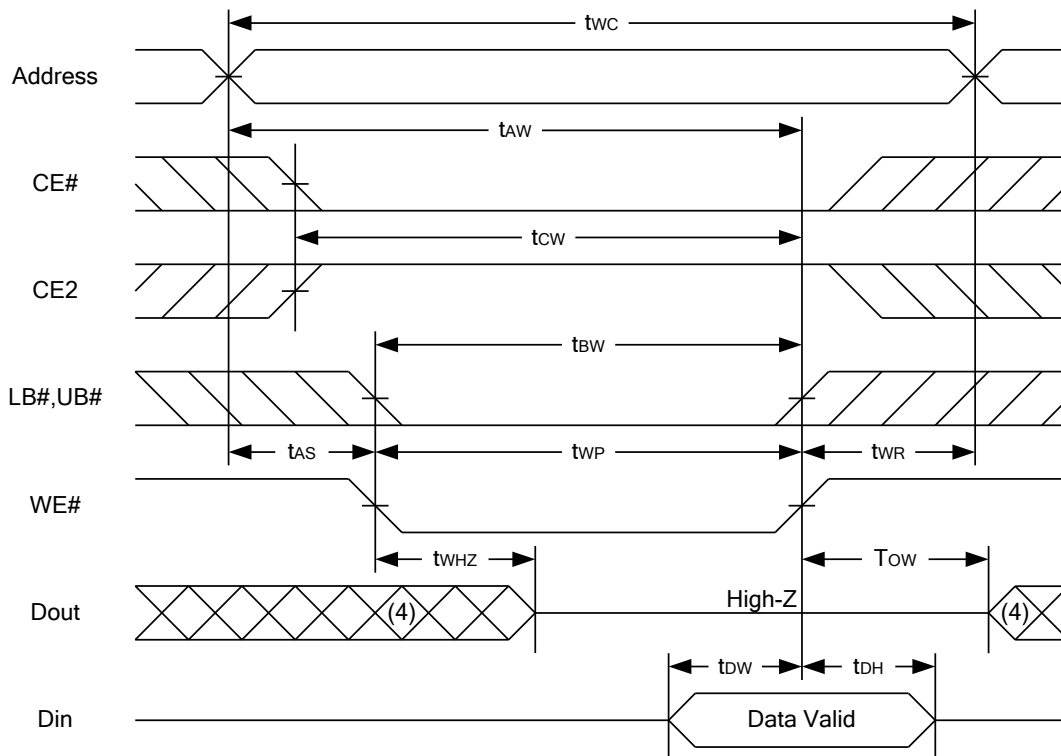
WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)
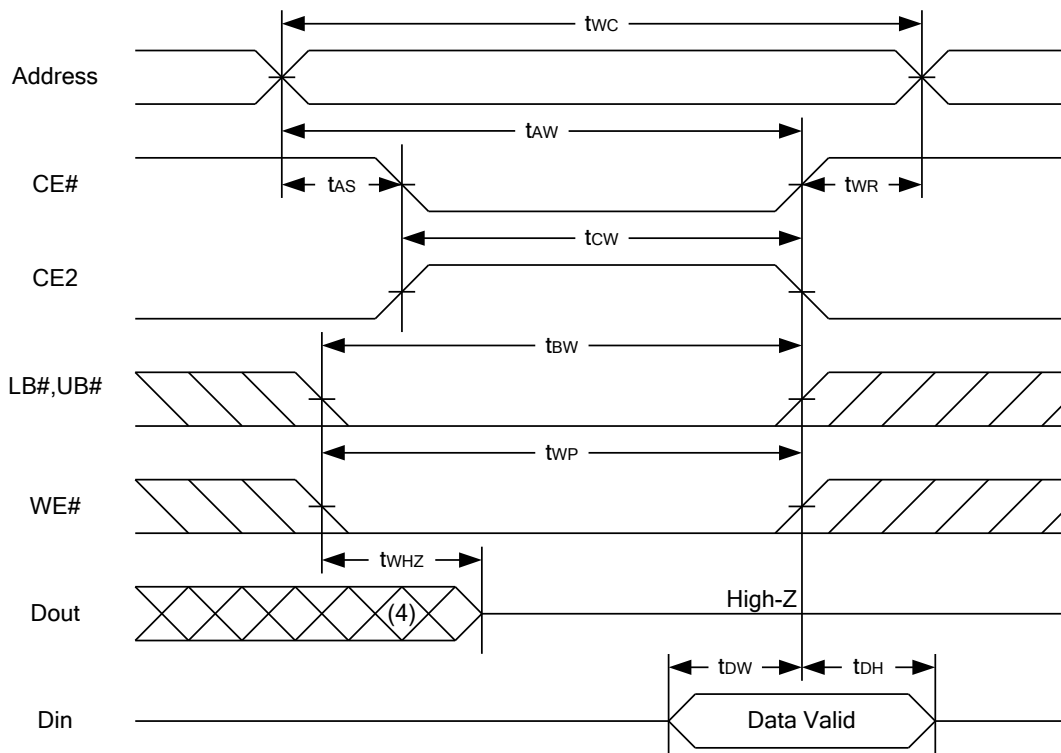
WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)
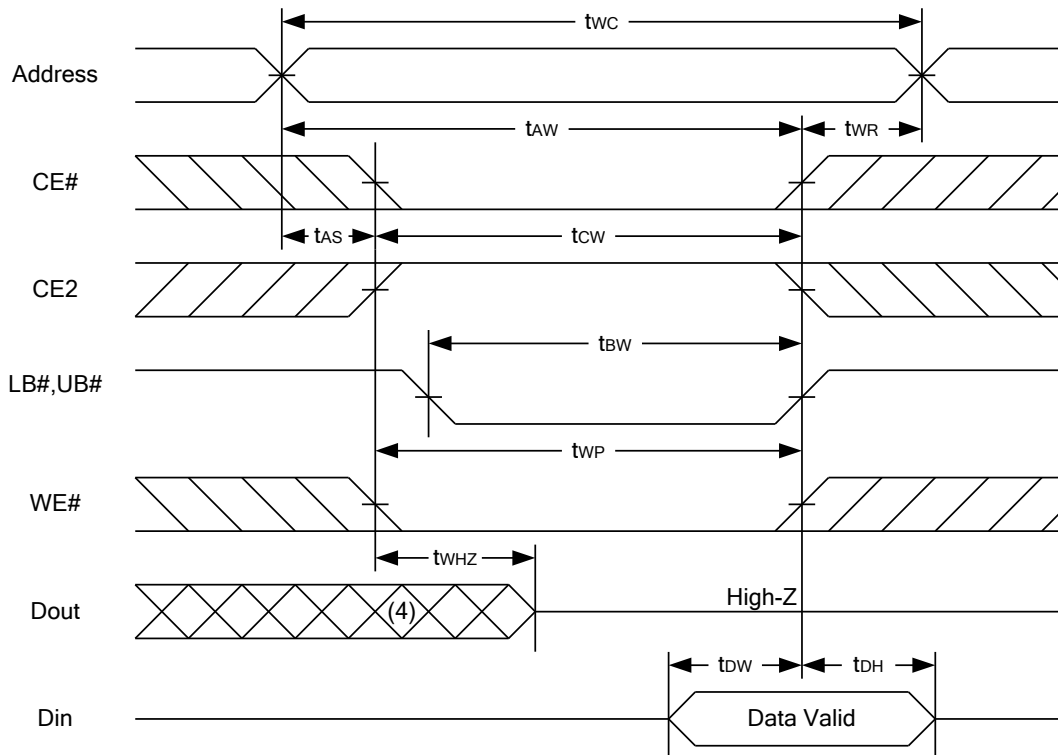
Notes :
1. WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

| PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_DR	CE#≧Vcc - 0.2V or CE2≦0.2V		1.2	-	3.6	V
Data Retention Current	I_DR	Vcc = 1.2V	-SL	-	8	80	µA
		CE# ≧Vcc-0.2V or CE2≦0.2V other pins at 0.2V or Vcc-0.2V	-SLI	-	8	120	µA
Chip Disable to Data Retention Time	t_CDR	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_RC*	-	-	ns

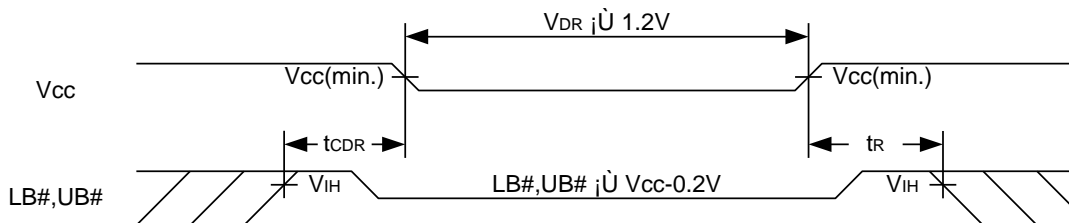t_RC* = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)
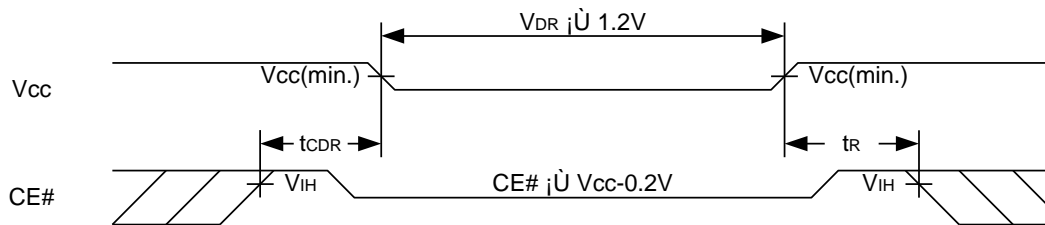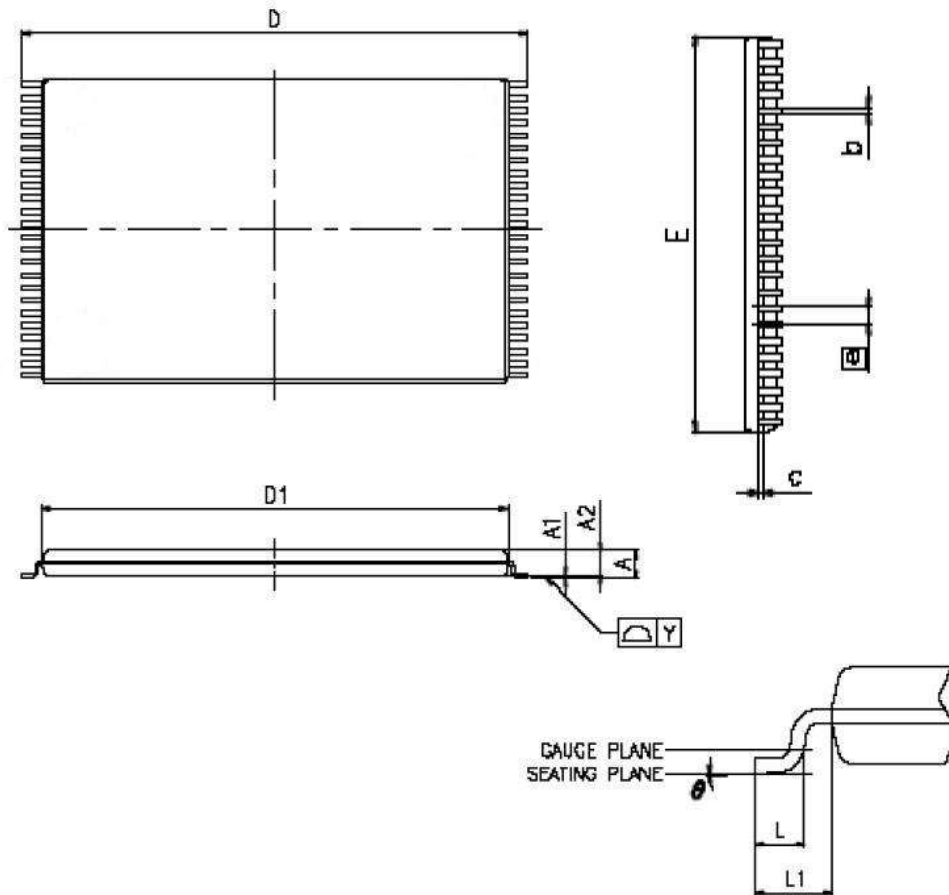

Low Vcc Data Retention Waveform (2) (CE2 controlled)
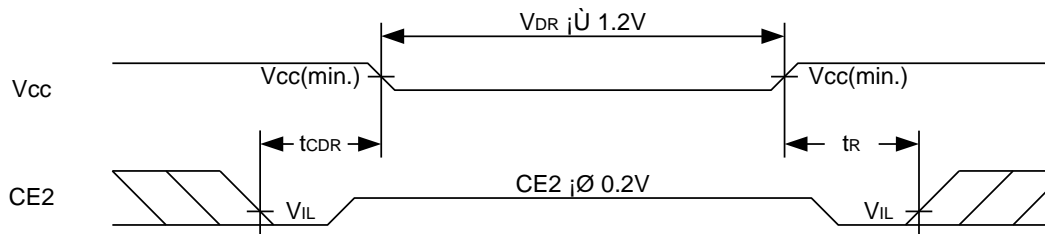
Low Vcc Data Retention Waveform (3) (LB#, UB# controlled)

Alliance Memory, Inc.

PACKAGE OUTLINE DIMENSION

48-pin 12mm x 20mm TSOP-I Package Outline Dimension

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	–	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
L1	–	0.80	–
Y	–	–	0.10
θ	0°	–	5°

NOTES:
1 JEDEC OUTLINE : MO-142 DD
2. PROFILE TOLERANCE ZONES FOR D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUN MATERIAL CONDITION DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C3216-55TIN	2050 x 16	2.7V – 3.6V	48pin TSOP I	Industrial ~ -40°C - 85°C	55

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