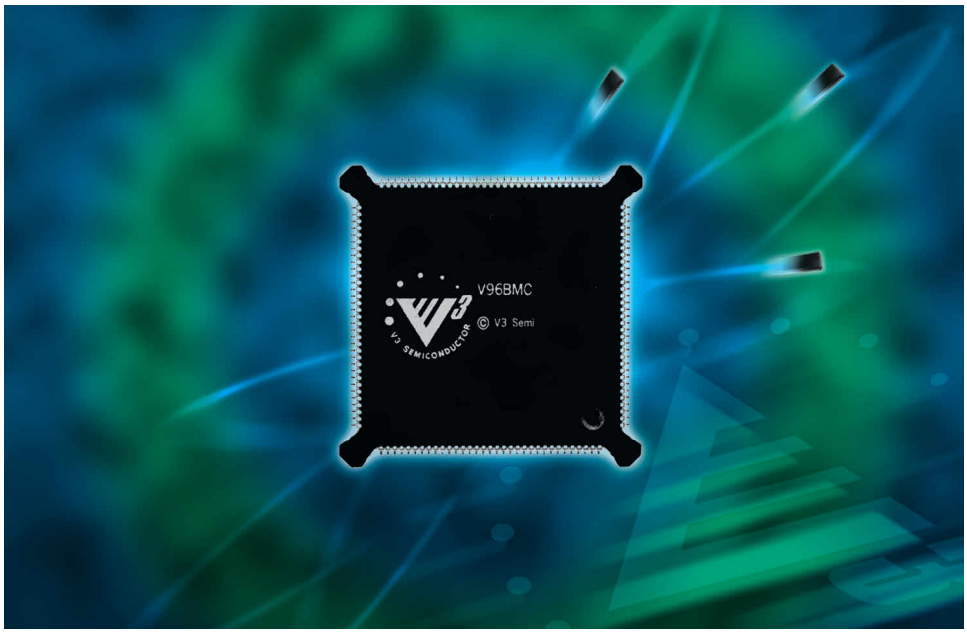
V96BMC

HIGH PERFORMANCE BURST DRAM CONTROLLER

For Intel® i960® Cx/Hx/Jx and IBM® PowerPC 401™ Gx Processors

- Direct interface to Intel® i960® Cx/Hx/Jx and IBM® PowerPC 401™ Gx processors
- Achieves SRAM performance using DRAM
- Supports up to 512 Mbytes of DRAM
- 3.3 V DRAM interface support
- Interleaved or non-interleaved operation
- Supports symmetric and non-symmetric arrays
- Operational parameters configured via software
- Integrated page cache management
- 2 Kbyte burst transaction support
- On-chip memory address multiplexer/drivers
- Two 24-bit counters/timers
- 8-bit bus watch timer
- Auto-refresh
- Up to 40 MHz operation
- Low-cost 132-pin PQFP package



The V96BMC Burst DRAM Controller provides all aspects of DRAM control for high-performance systems. It includes all the DRAM access protocols, buffer control signals, multiplexed address signals, and bus timing resources required to work with FPM/EDO DRAMs. By using the V96BMC, system designers can replace expensive FPGAs and conserve valuable board space. The V96BMC also provides dedicated power and ground rails to work with 3.3 V DRAM modules.

The V96BMC supports a total DRAM memory subsystem size of 512 Mbytes. The array may be organized as 1 or 2 leaves of 32 bits each. Standard memory sizes of 256 Kbit to 64 Mbit are supported, and 8-, 16-, and 32-bit accesses are allowed. The V96BMC achieve static RAM performance using dynamic RAM by taking advantage of fast page mode or EDO DRAM and row comparison logic.

The processor interface of the V96BMC implements the bus protocol of the i960® Cx/Hx/Jx and the PowerPC 401™ processors. The pin naming convention on the V96BMC is the same as the i960®—simply connect like-named pins to create the interface.

The V96BMC supplies the control signals needed for external data path buffer components. The use of multi-mode control signals gives the designer the flexibility to select buffer components that are optimized for price/performance. Most standard buffers can be used without additional external logic.

The V96BMC provides an 8-bit bus watch timer to detect and recover from accesses to unpopulated memory regions. Two 24-bit counters/timers can supply an external interrupt signal at a constant frequency relative to the system clock.

The V96BMC is packaged in a low-cost 132-pin PQFP package and is available in 33 MHz and 40 MHz speed grades.

SEMICONDUCTOR
THE EMBEDDED INTELLIGENCE COMPANY

COST EFFECTIVE SOLUTIONS THAT SIMPLIFY EMBEDDED SYSTEM DESIGN

Development Tools

To help accelerate development and reduce time-to-market, V3 Semiconductor provides simulation models, software tools, reference designs, and evaluation boards. This allows the developer to concentrate on product differentiation.

V3 Semiconductor offers a unique, interactive technical support system. V3Help assists designers with the challenges they face throughout development, from initial concept through prototype and production.

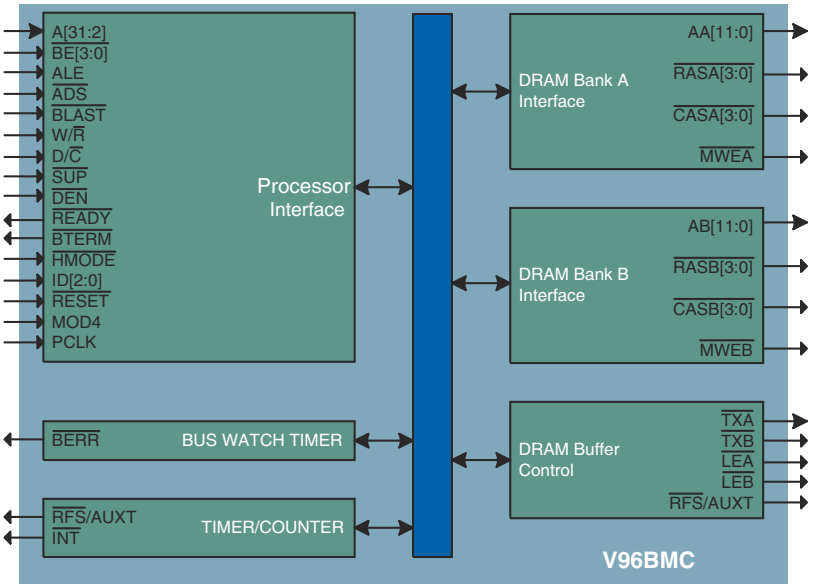
Applications of the V96BMC

- Networking systems
- Office automation products

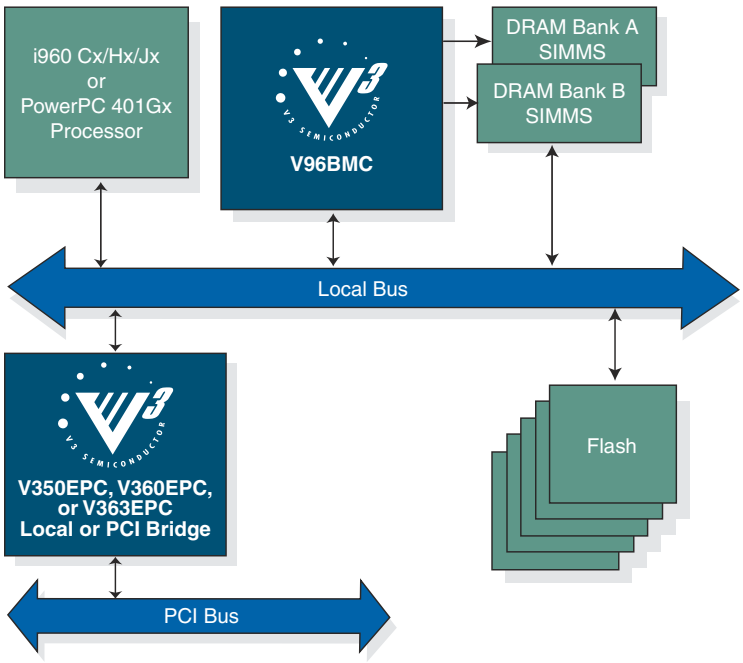
Product Ordering Information

V96BMC-33LPD	**V96BMC** High Performance Burst DRAM Controller, 33 MHz
V96BMC-40LPD	**V96BMC** High Performance Burst DRAM Controller, 40 MHz

V96BMC Block Diagram



V96BMC Example Application



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