APR 9 1992

V96BMC

Burst Memory Controller
Advance Information

i960 CA Support Product!

Features

- Interfaces directly to the i960 CA
- Manages Page Mode Dynamic Memory devices
- Supports DRAMs from 256Kb to 64Mb.
- Manages Instruction and/or Data Memory
- Includes 24 Bit Counter/Timer, 5 Bit Bus Watch Timer
- On Chip Memory Address Multiplexer/Drivers
- "Same Row" Address Compare
- Software-Configured operational parameters
- Programmable Bank Size and Location
- High-Speed/Low Power CMOS Technology

Description

The V96BMC Burst Memory Controller is a single chip device designed to simplify the implementation of burst access in high performance systems using the i960 CA SuperScalar Embedded Processor.

The extremely high instruction rate achieved by this processor places extraordinary demands on memory system designs if maximum throughput is to be sustained and costs minimized.

Static RAM is the most obvious solution to implementing a high speed memory system. However, the high cost and low density of these devices make them an expensive and space consumptive solution.

Dynamic RAMs are an attractive alternative for their high density and low cost. The impediment to using DRAM is their relatively slow access times and more complex control circuitry.

However, when operated in page mode, dynamic RAMs behave more like static memories. Properly managed, they can yield access times rivaling those of fully static RAMs.

The function of the V96BMC is to interface the page mode access protocol of dynamic RAMs with the more general burst access protocol supported by the i960 CA. The device manages single or double banked arrangements of dynamic RAMs such that when burst accesses are permitted data can be read, or written, at the rate of one word per system clock cycle.

i960CA system integration is further enhanced by the chips 24 bit timer which can be used to generate clock interrupts. A 5 bit bus watch timer insures that an external access will not freeze the processor for lack of data READY.

Packaged as a 132 pin plastic QFP, the V96BMC drives memory arrays directly, thus minimizing design complexity and package count.

Fig 1 - Typical System Configuration

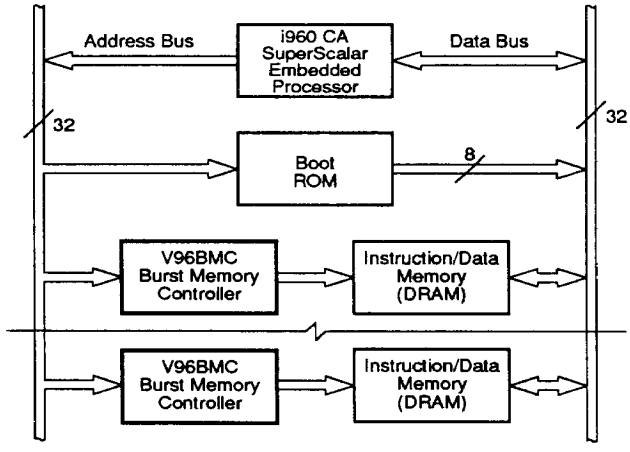

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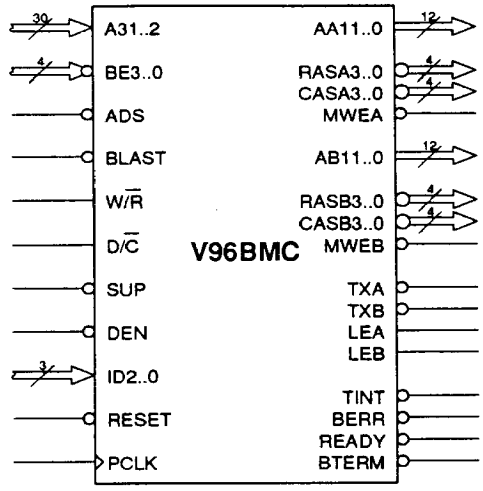
Fig 2 - Logic Symbol



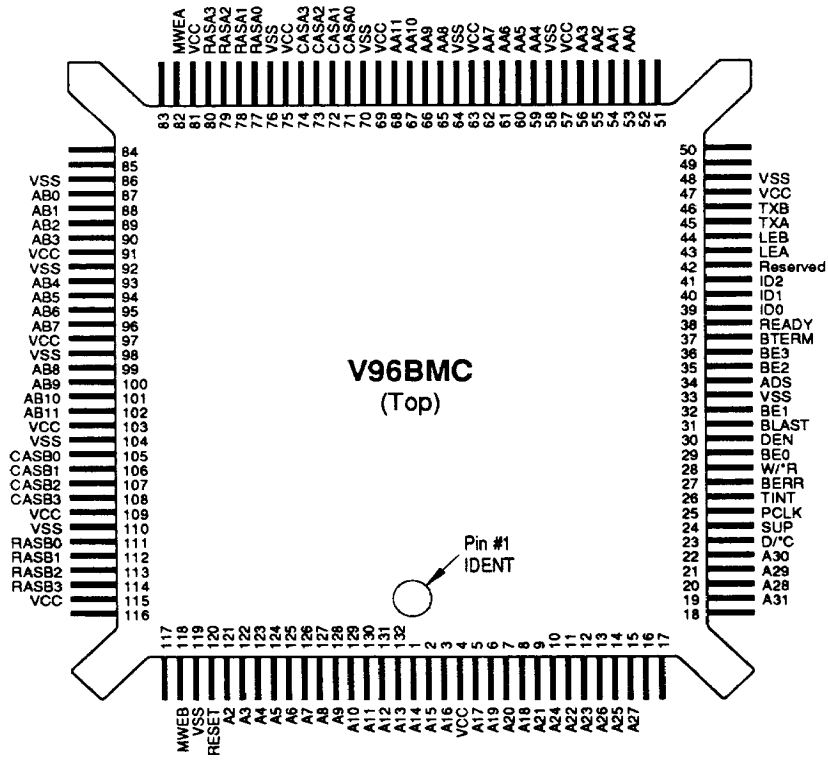


Fig 3 - Connection Diagram

Pin Designation 132 Pin PQFP

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	A14	44	LEB	91	VCC
2	A15	45	TXA	92	VSS
3	A16	46	TXB	93	AB4
4	VCC	47	VCC	94	AB5
5	A17	48	VSS	95	AB6
6	A19	53	AA0	96	AB7
7	A20	54	AA1	97	VCC
8	A18	55	AA2	98	VSS
9	A21	56	AA3	99	AB8
10	A24	57	VCC	100	AB9
11	A22	58	VSS	101	AB10
12	A23	59	AA4	102	AB11
13	A26	60	AA5	103	VCC
14	A25	61	AA6	104	VSS
15	A27	62	AA7	105	CASB0
19	A31	63	VCC	106	CASB1
20	A28	64	VSS	107	CASB2
21	A29	65	AA8	108	CASB3
22	A30	66	AA9	109	VCC
23	D/C	67	AA10	110	VSS
24	SUP	68	AA11	111	RASB0
25	PCLK	69	VCC	112	RASB1
26	TINT	70	VSS	113	RASB2
27	BERR	71	CASA0	114	RASB3
28	W/R	72	CASA1	115	VCC
29	BE0	73	CASA2	118	MWEB
30	DEN	74	CASA3	119	VSS
31	BLAST	75	VCC	120	RESET
32	BE1	76	VSS	121	A2
33	VSS	77	RASA0	122	A3
34	ADS	78	RASA1	123	A4
35	BE2	79	RASA2	124	A5
36	BE3	80	RASA3	125	A6
37	BTERM	81	VCC	126	A7
38	READY	82	MWEA	127	A8
39	ID0	86	VSS	128	A9
40	ID1	87	AB0	129	A10
41	ID2	88	AB1	130	A11
42	Reserved	89	AB2	131	A12
43	LEA	90	AB3	132	A13

Note In order for the switching characteristics of this device to be guaranteed, it is necessary to connect all of the power pins (Vcc, Vss) to the appropriate power levels. The use of low impedance wiring to the power pins is required. In systems using the i960 CA with its attendant high switching rates, multi-layer printed circuit boards with buried power and ground planes are required.

Pin Description; i960 CA Interface

The following pins have the same function as their counterparts on the i960 CA and are designed to be connected directly to the i960 CA Bus Interface.

A2-31 Address Bus (Input)
The address bus input is a byte address which controls the memory access address. The V96BMC can be software configured to any memory block address within the 4 Gbyte address range.

ADS Address Strobe (Input; Active Low)
This input is used to indicate that a new valid address is asserted on the address bus.

BE0-3 Byte Enable (Input; Active Low)
The byte enable inputs are used to enable the CAS signals on a per-byte basis to allow byte write support.

BLAST Burst Last (Input; Active Low)
Indication from the processor that the last cycle of a sequential burst is in progress.

D/*C Data/*Code (Input)
This input signals that an access is a data access (High) or code access (Low).

DEN Data Enable (Input; Active Low)
The Data Enable input is monitored by the Bus Watch Timer to detect access to unimplemented address regions. (External READY enabled but not generated)

SUP Supervisor (Input; Active Low)
Indicates that the current cycle is a supervisory mode access.

READY Data Ready (Output; 3-State; Active Low)
The READY output is used to signal that data on the processor bus is valid (Read) or that the memory system is finished with data from the processor (Write).

W/*R READ/*WRITE (Input)
This input indicates whether data is being transferred to the data bus (**W/*R** low) or to the memory array (**W/*R** high).

RESET Reset (Input; Active Low)
This input initializes the V96BMC to its reset value. Following reset the chip is ready to accept the software configuration information.

PCLK System Clock (Input)
This input is used to synchronize the V96BMC to the i960CA processor interface.

BERR Bus Error (Output; Active Low)
When enabled, a Bus Error is generated if DEN is asserted for longer than a pre-determined number of cycles.

TINT Timer Interrupt (Output) (Output; 12mA; Active Low)
The Timer Interrupt output is asserted periodically by the programmable 24 Bit counter. The output can be programmed for both edge and level sensitive interrupt modes.

ID0-2 Chip ID (Input)
These inputs control the base address of the chip's configuration registers. Each V96BMC in a system should have a unique binary code asserted at these pins so that each controller will have a unique base address for it's configuration registers.

Pin Description; Memory Interface

The V96BMC is designed to drive a memory array organized as 2 banks each of 32 bits. The address and control signals for the memory array are output through high current drivers in order to minimize the propagation delay due to memory input impedance and trace capacitance. External array drivers are not required. The address and control signals, however, must be externally terminated.

A(A,B)0-11 Multiplexed Addresses (Output; 24mA)
These two buses transfer the multiplexed row and column addresses to the memory array banks A and B respectively.

RAS(A,B)0-3 Row Address Strobes (Output; 12mA, Active Low)
These signals are strobes that indicate the existence of a valid row address on A(A,B)0-10. These signals are to be connected to the two interleaved banks of memory. Four are assigned to each bank.

CAS(A,B)0-3 Column Address Strobe (Output; 12mA, Active Low)
These signals are strobes that indicate a valid column address on A(A,B)0-10. A set of each of these (A,B) are assigned to each memory bank, and within each set, one is assigned to each byte of the 32 bit memory.

MWE(A,B) Memory Write Enable (Output; 24mA, Active Low)
These signals are the write strobes for the DRAM memories. Although they are logically identical, one is supplied for each of the two banks of memory so that loading effects can be minimized.

Pin Description; Buffer Controls

Buffer control signals are provided to simplify the interconnection of the DRAMs data signals with the i960 CA data bus. The buffer controls also provide for a flexible choice of buffer types including simple buffers such as "245"s, latching buffers such as "543"s and registered types ("646"s).

The following buffer control outputs are multi-mode signals. The signal names, as they appear on the logic symbol, are the default signal names (Mode=0). A more complete description is presented in the configuration section.

TX(A,B) Data Bus Transmit A and B (Output; Active Low)

These outputs are used during read cycles to enable data from the individual banks of memory to drive the data bus.

LE(A,B) Data Bus Latch Enable A and B (Output; Active High)

These outputs are used to enable transparent latches to latch data from the Processor data bus to each bank of memory during a write cycle. In modes 00 and 01 the latch outputs follow the timing of CAS and are intended to be used to separately latch data for both the A and B banks of memory. In modes 10 and 11 the outputs are combined to provided a common signal for use with buffers driving data to both banks of memory.

FUNCTIONAL DESCRIPTION

Product Overview

The V96BMC is designed to simplify the interface between the i960 CA high-speed external bus and dynamic memories. This integrated circuit responds to both basic access and burst access modes of the i960 CA, and handles all required address decoding and multiplexing for the DRAM memory array. In addition, the V96BMC automatically generates refresh cycles to the memory array. Software configuration is used to setup the memory block address, refresh rate, bus buffer control type and DRAM memory chip size parameters for the memory block.

If two or more V96BMCs are used to implement an i960 CA memory sub-system, the processor can access one memory block as code and the other as data. Typically this results in a higher hit rate of the "same row" detection feature resulting in improved performance. However, only a single V96BMC controller is required for a fully functional system with performance close to that of a dual controller system.

System Interface

The V96BMC connects directly to the i960 CA address bus and control signals. The interface handles basic and burst mode access according to the i960 CA bus specification and requires no external bus interface logic. Thus, it avoids the propagation delays and signal skews that can detract from system performance and increase system complexity.

Memory Interface

The V96BMC directly drives an array of DRAM I.C.s which can support fast page mode access. The array is organized as 2 banks of 32 bits each. The devices supported are all the standard memory sizes from 256Kbit to 64 Mbit. Selection of the device in use is done via software.

During burst access, the V96BMC executes interleaved page mode access to the 2 banks. This allows the memory to run at the full processor speed of 1 memory cycle per processor cycle (0 wait state). For data access, the V96BMC controls the memory as four independent 8 bit bytes in order to allow 8, 16 and 32 bit access. Each memory byte is driven by a separate CAS strobe enabled according to the processor's byte enable signals.

The V96BMC allows for flexibility in the control of data buffers for the memory array. Propagation delay is minimized by providing these controls directly, and by allowing the control strategy to be software programmable. For example: 74FCT245, 74FCT543, 74FCT646, 74FCT853 or 74FCT861 bus buffers may be used without external 'glue' circuitry.

Configuration

Each V96BMC in a system has a configuration register which is mapped into a 8K space in the processor's 32 bit address range. The actual base address of the 8K space is determined according to the state of the ID0-2 pins on the V96BMC. Each V96BMC in a system should have a unique binary code asserted at these pins so that each one can be configured with a unique configuration word. The 8K address space of the configuration register is subdivided into 8 - 1K regions each representing 8 bits of the 64 bit configuration word. Each byte of the configuration word is loaded with the value contained in the low 8 bits of the physical address bus (A2..9) when a supervisor mode write cycle is performed within one of the 1K regions. Consequently, it is the lower bits of the address bus which are used as "data" for the configuration. In this way the processor's data bus doesn't require connection to the V96BMC thus saving component pins. V96BMC devices must be configured before memory access is attempted.

ID2	ID1	ID0	Base Address
0	0	0	FF0F0000
0	0	1	FF0F2000
0	1	0	FF0F4000
0	1	1	FF0F6000
1	0	0	FF0F8000
1	0	1	FF0FA000
1	1	0	FF0FC000
1	1	1	FF0FE000

Table 1. V96BMC Configuration Base Address as a Function of ID Map.

The configuration register itself is depicted in figure 4. Each of the configuration fields is described in the following section. A configuration example concludes the discussion.

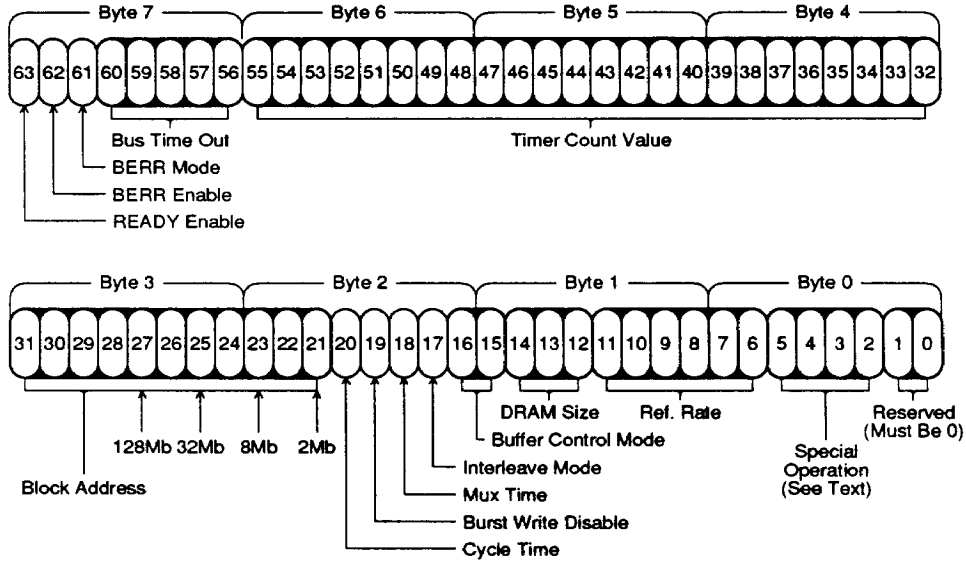


Fig 4 - V96BMC Configuration Word

Block Address

Once configured, a V96BMC only responds to addresses within the configured block address range. The programmed value corresponds to the starting address of the block, while the size of the block is determined by the DRAM size control bits. For example, if 1M x 1 DRAM I.C.s are selected, the memory block size is 8M bytes and is always located on an 8M byte boundary. Figure 4 shows the least significant bit of the block address for each block size.

Cycle Time

In order to maximize the choice of memory device speeds that may be used with various system clock rates, the V96BMC can be configured such that the Row Address Strobe (RAS) period lasts for either 3 or 4 clock periods for a basic access. When cleared to "0", configuration bit 20 indicates that 3 clock cycles (2 wait states) are to be used for a basic access (2-0-0-0 wait states for burst), when set to "1", 4 are required (3 wait states for a basic access 3-0-1-0 for burst). Calculation of the number of cycles required is detailed in the V96BMC Application Guide.

Burst Write Disable

Bit 19 of the configuration can be set to "1" to disable burst write cycles. The V96BMC accomplishes this by asserting the BTERM signal to force a new address strobe for the next datum of the burst. This feature is provided so that systems employing no latching buffers between processor and memory are possible. Without latches to provide data hold time to the DRAM, the needed hold time is achieved by converting a burst into a basic access. In a basic access the data is held until the end of the CAS strobe which provides plenty of hold time for the DRAM.

Mux Time

Bit 18 of the configuration register controls the time at which the memory address switches from row to column address. This allows the designer to control Row Address Hold time so that the slowest memory can be used for a range of clock speeds. Seting Bit 18 to "1" yields the maximum row address hold time. When bit 18 is clear, the row address hold is shortened in favor of additional column address setup time.

Interleave Mode

In some systems it may be desirable to allow operation with only a single bank of memory. In such cases the interleave mode bit is programmed to "1". If a second bank of memory is later added then this mode bit can be programmed to "0" for normal interleave operation allowing peak performance. In non interleave mode a burst access contains either 2-1-1-1 wait states (bit 20=0) or 3-2-2-2 (bit 20=1).

Buffer Control Modes

The combination of programmable Cycle time and burst write enable/disable permit the system designer to trade memory device speed and organization in order to optimize system performance, cost, and storage capacity. This flexibility is further enhanced by providing multiple methods of buffering the memory sub-system and the i960 CA bus interface.

Table 2 - Interpretation of the Buffer Control Signals for Various Control Modes

Mode Bits	Signal 1	Signal 2	Signal 3	Signal 4
00	TXA	TXB	LEA	LEB
01	CEA	CEB	LEA	LEB
10	TX	BankB/*A	LEA	LEB
11	CE	BankB/*A	LEA	LEB

Note: The mode 00 signal names are the defaults used for reference purposes.

The transfer of Data from the memory sub-system to the i960 bus occurs through buffers controlled by the V96BMC. Two signals provide latch enable controls (LEA, LEB) for transparent latches for use during data transfers from the i960 CA to memory (write cycles).

The functions performed by the buffer control signals change according to programmed mode. Table 2 presents these signals using names that are function derived. Signals containing TX are Buffer transmit controls which are typically used with buffers that have output enables (transmit - relative to the memory system). Buffers such as 74FCT245 or 74FCT646 which have direction and enable pins are controlled with

a CE (chip enable) signal (modes 01 and 11).

Signals ending with A or B are specific to one or the other of the two interleaved banks of memory controlled by the V96BMC; signals without suffixes apply to both banks. The signal BankB/*A, required in some configurations, indicates which DRAM memory bank will be selected next.

The memory buffer strategy required will depend on the type of DRAMs being used (bit wide vs. nibble wide components), the access time of these memories, the desired cost/performance trade-off, and the system clock speed. Table 3 presents some of the possible configurations with the corresponding mode settings. For a comprehensive discussion of the selection of a buffer strategy, please refer to the V96BMC Application Guide. This document expands the rationale of the selection process and presents specific application examples and circuit diagrams.

Table 3 - Possible V96BMC Memory/Buffer Configurations

	Buffer Type	DRAM Type	Wait States		Buffer Mode
			Write	Read	
1	74FCT245	Nibble	2-4-4-4*	2-0-0-0	Mode 3
2	74FCT245	Bit	2-4-4-4*	2-0-0-0	Mode 1
3	74FCT646	Nibble	1-0-0-0	2-0-0-0	Mode 3
4	74FCT543	Bit	1-0-0-0	2-0-0-0	Mode 0
5	Am29C983	Bit	1-0-0-0	2-0-0-0	Mode 2
6	None	Nibble	2-4-4-4*	2-0-0-0	Mode 2,3

DRAM Size

This three bit field, bits 12-14, configures the V96BMC for the correct memory address size, and hence total memory block size. Note that the memory in both banks of a block are required to be of the same size and organization in order for correct operation to occur. Table 4 lists the supported device sizes.

Table 4 - Size code settings, DRAM Density and Address range size

Memory Size Code	Memory Block Size	Max Banks	Memory Types
0 0 0	2M	1	256Kx1
0 0 1	8M	1	1Mx1
0 1 0	32M	1	4Mx1
0 1 1	128M	1	16Mx1, 16Mx4
1 0 0	2M	4	64Kx4
1 0 1	8M	4	256Kx4
1 1 0	32M	4	1Mx4
1 1 1	128M	4	16Mx4

Refresh Rate

The system clock frequency is used to derive the period of DRAM refresh cycles. The refresh rate is given by (PCLK clock frequency) / (16 x (programmed value+1)). For example, if the system clock is 25MHz and the programmed value is 24 (0x18), the V96BMC will execute the 256 refresh cycles for a 256K DRAM in 4.096 milliseconds. Bit 11 of the configuration word is the MSB of the frequency field while bit 6 is the LSB. The refresh algorithm employed by the V96BMC guarantees the time for complete device refresh, however, the time for individual row refreshes may be held off so as not to needlessly preempt bursts in progress.

Special Operations

A 4 bit field in byte 0 of the configuration is used to selectively enable/disable functions of the V96BMC which the user may want to access "on the fly". Consequently any, access to byte 0 of the configuration register in which any of the "special operation" bits are asserted will affect only a single parameter of operation. In this way it is possible to access the special operations without disturbing other parameters (such as the lower bits of the refresh rate). Other bytes of the configuration are typically only modified following a system reset.

Config. Bits				Operation
5	4	3	2	
0	0	0	0	No Operation (Access other Configuration Bits - 0-2, 6, 7)
0	1	0	0	Instruction Access Row Compare Disable (Default)
0	1	1	0	Instruction AccessRow Compare Enable
0	1	0	1	Data Access Row Compare Disable (Default)
0	1	1	1	Data AccessRow Compare Enable
1	0	0	0	Acknowledge Timer Interrupt
1	0	1	0	Enable Timer Output for Level Sense Interrupt
1	1	0	0	Disable All Timer Interrupts
1	1	1	0	Enable Timer Output for Edge Sense Interrupt

Row Compare Enable/Disable

The Row Compare feature of the V96BMC provides fewer wait states for successive access, that are within a 2K address range, by not re-asserting the RAS (Row Address Strobe) of the DRAM. Instead, only the appropriate CAS (Column Address Strobe) signals are asserted resulting in higher speed access. After system RESET, the V96BMC has the row detection feature disabled. The feature can be enabled/disabled independantly for both instruction and data access. The decision to enable/disable row compare for I/D will depend on the number of V96BMCs in a system in addition to the code being executed. Systems employing 2 V96BMCs will generally benefit by placing data in memory controlled by one of the V96BMCs with Data Row Compare enabled. Instruction execution should then take place out the second V96BMCs memory with Instruction Row Compare enabled.

Timer Functions

The 24 bit timer is intended as a simple interrup generator which divides PCLK by a programmable amount and auto-reloads on terminal count. It is not possible to read the contents of the timer since the data bus is not connected to the V96BMC. The timer is initially disabled following a RESET and should have the Timer Count Value Programmed (Bytes 5-6 of the configuration register) before it is enabled. Two modes of operation are possible: edge triggered interrupt or level sense interrupt with acknowledge. Edge interrupt mode generates a one cycle pulse when terminal count is reached (Low for one cycle). In level interrupt mode, the output is asserted low on terminal count and de-asserted by accessing the "Acknowledge Timer Interrupt" instruction using the special operations of configuration byte 0.

Bus Watch Timer

When enabled, the 5 bit bus watch timer is used to monitor a bus access in progress to prevent bus "freeze" when a peripheral fails to return a READY. This is accomplished by monitoring the DEN signal from the i960CA. If the DEN signal is asserted for longer than the number of cycles programmed into the "Bus Time Out" bits of the configuration register (Byte 7) then one or both of the following actions can be enabled to occur: assert the READY signal (configuration bit 63=1) and/or generate an interrupt on the BERR output of the V96BMC (configuration bit 62=1). Like the timer interrupt, the interrupt can be programmed for pulsed operation for edge triggered interrupts (configuration bit 61=0) or require an acknowledge (configuration bit 61=1). An acknowledge is accomplished by reading configuration register 7 (the data is not used).

Interconnect Details

Interconnection between the V96BMC and the i960 CA processor is accomplished by directly connecting the pins with the same names. The READY output from the V96BMC can be connected directly to the READY input of the processor. A pull up resistor is required to keep READY de-asserted when it is in its high impedance state. If multiple processor peripherals are connected to the common READY input to the processor, then totem pole drivers cannot be used. Likewise, "open collector" drivers should also not be used since they rely entirely on a pull up resistor to de-assert them. With the high clock rates of the i960 CA, the rise time of the passively pulled up signal will not guarantee de-assertion in time for the next clock edge resulting in a false READY state. Consequently, all logic driving the READY signal should use 3-state drivers in such a way that the signal is actively de-asserted prior to the driver being placed in its' high impedance state. Such is the case with the V96BMC. Alternately, all sources of READY can be combined with a multiple input gate to drive the processor's READY.

Application

The ease with which the V96BMC may be integrated into a system design is illustrated in the diagram in Figure 5. The system shown supports an i960 CA with between 2 and 128 Mbytes of memory (depending on the storage devices selected) managed by a single V96BMC. This specific example accommodates 1Mx1, 4Mx1 or 16Mx1 devices.

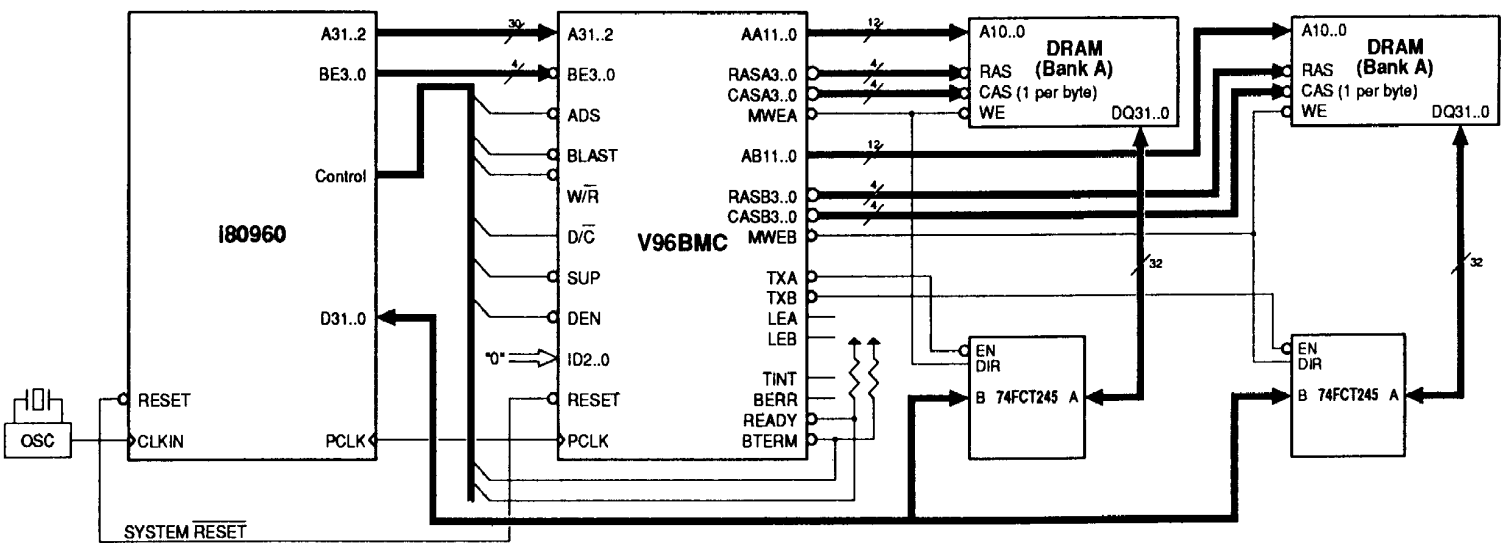


Figure 5. Possible System Interconnection using V96BMC.

Timing Parameters

Interface Timing

The V96BMC interface to the i960 CA has been designed for direct interconnect. Normally it is not necessary to place other logic devices between the processor, V96BMC, and memory with the exception of data bus buffers. The introduction of intermediate address or control signal buffers can result in skews or delays that will require that the system clock frequency be derated for operation under worst case conditions.

Refresh Timing

Figure 6 details the timing of the Row only refresh performed by the memory controller. The shaded section represents the case that configuration bit 20 is set to "1" (RAS Time). When bit 20 is cleared to "0" then the shaded cycle is not present resulting in a 3 cycle RAS strobe.

Simple Access Timing

The V96BMC can return data to the processor in only 3 or 4 clocks for a basic access (2 or 3 wait states) depending on the mode chosen (Configuration Bit 20). If multiple access cycles are requested back to back then the BMC will pause for a minimum of 2 clocks between RAS cycles to insure that the RAS precharge time is met resulting in 5 or 6 clocks between successive simple cycles (depending on Configuration bit 20).

All access modes begin their cycle in the same fashion as a basic access. Figure 7 shows the timing relationship between the system clock, processor control signals and V96BMC outputs. All V96BMC outputs are derived synchronously with the exception of t_{ARA} (processor address to memory address delay). The shaded section in Figure 7 represents the extra cycle inserted when the configuration register is initialized with bit 20 cleared.

Burst Access Timing

When a 4 word burst access is established, the V96BMC generates the signal sequence of Figure 8. The burst sequence can be shortened by asserting BLAST earlier than indicated in the diagram. Note that a burst access begins in the same manner as a basic access. Consequently the timing parameters from Figure 6 can also be applied to Figure 8.

Figure 6. Refresh Timing.

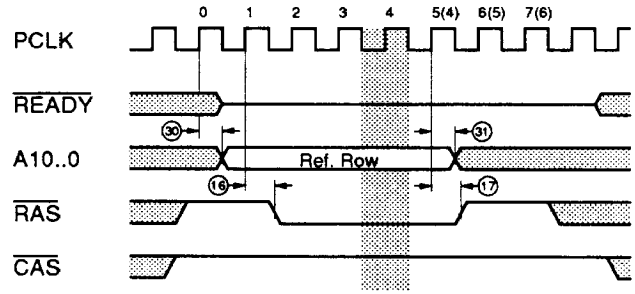


Table 5 - Timing Parameters

#	Symbol	Description	16 MHz		25MHz		33MHz		40MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{ADSU}	Address Strobe setup time	14		12		9				ns.
2	t_{ADH}	Address Strobe hold time		3		3		3			ns.
3	t_{SU}	Synchronous Input Setup	14		12		9				ns.
4	t_{H}	Synchronous Input Hold		3		3		3			ns.
5	t_{BLSU}	BLAST Input Setup	16		13		11				ns.
6	t_{BLH}	BLAST Input Hold		3		3		3			ns.
7	t_{RZH}	READY 3-state to valid delay relative to *PCLK		31		26		21			ns.
8	t_{RHL}	READY synchronous assertion delay		28		23		18			ns.
9	t_{RLH}	READY synchronous de-assertion delay		27		22		18			ns.
10	t_{RHZ}	READY valid to 3-state delay relative to *PCLK		29		24		19			ns.
11	t_{ARA}	Address Input to Row Address output delay ①		23		19		15			ns.
12	t_{RAH}	*PCLK or PCLK to row address hold		40		33		26			ns.
13	t_{CAV}	*PCLK or PCLK to column address valid ①		38		31		25			ns.
14	t_{CAH}	PCLK to column address hold	4		4		4				ns.
15	t_{DRAH}	DRAM row address hold ②	t_{M-4}		t_{M-4}		t_{M-3}		t_{M-3}		ns.
16	t_{RSHL}	PCLK to RAS asserted delay ①		29		24		19			ns.
17	t_{RSLH}	PCLK to RAS de-asserted delay ①		26		21		17			ns.
18	t_{CHL}	PCLK to CAS asserted delay ①		23		19		15			ns.
19	t_{CLH}	PCLK to CAS de-asserted delay ①		20		16		13			ns.
20	t_{BHL}	PCLK to Buffer Control asserted delay ①		26		21		17			ns.
21	t_{BLH}	PCLK to Buffer Control de-asserted delay ①	4	23	4	19	4	15			ns.
22	t_{BSV}	PCLK to Bank Select valid delay ①		26		21		17			ns.
23	t_{BSH}	PCLK to Bank Select hold time ①	4		4		4				ns.
24	t_{WEHL}	*PCLK to Write Enable asserted delay ①		31		25		20			ns.
25	t_{WELH}	PCLK to Write Enable de-asserted delay ①									ns.
26	t_{CAH}	*PCLK to Column address hold time ① (Burst)	5		5		4				ns.
27	t_{CAV}	*PCLK to Column address valid delay ①(Burst)		29		23		19			ns.
28	t_{LEHL}	*PCLK to latch enable assertion		23		19		15			ns.
29	t_{LELH}	PCLK to latch enable de-assertion		20		16		13			ns.
30	t_{RFA}	PCLK to Row Address Valid (Refresh)									ns.
31	t_{RFH}	PCLK to Row Address Hold (Refresh)									ns.

Signal output delays are measured relative to PCLK (except as indicated) using a 50 pF. load.

① Derate the given delays by 0.06 ns per pF. of load in excess of 50 pF.

② t_M = PCLK High duration when config. bit 18=0. t_M = PCLK cycle time = $^1/_{(PCLK\ frequency)}$ for config. bit 18=1.

Timing for Sample silicon

Figure 7 - Basic Access Timing

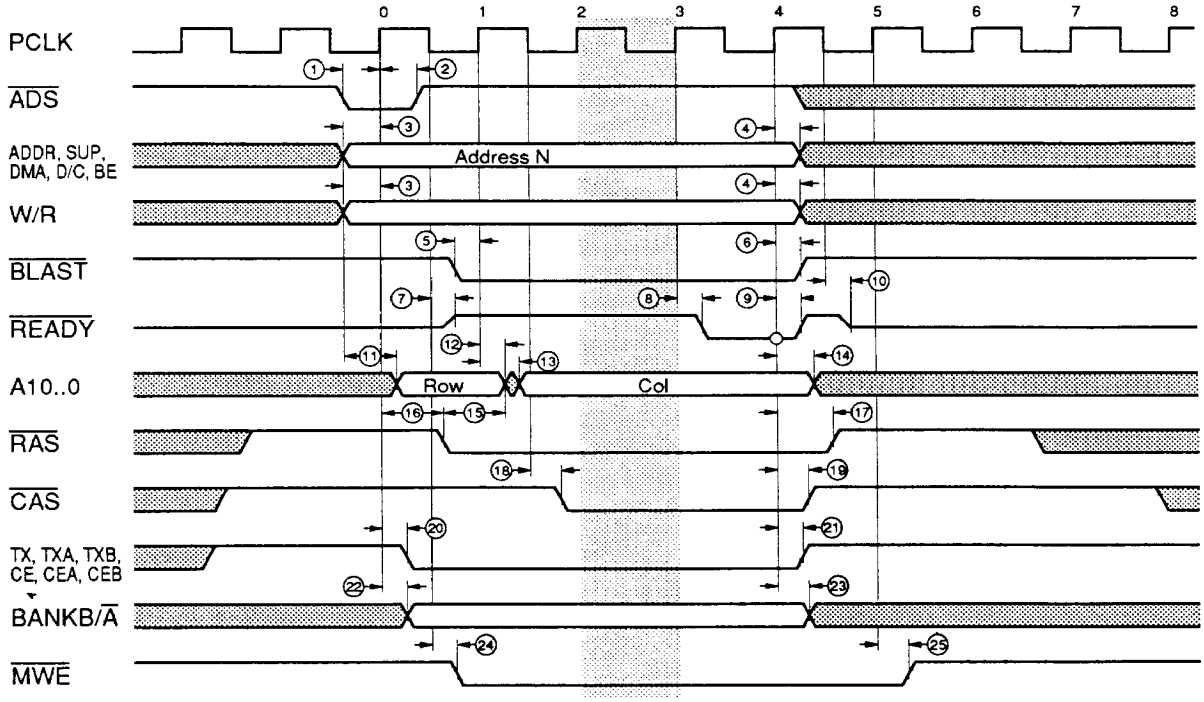
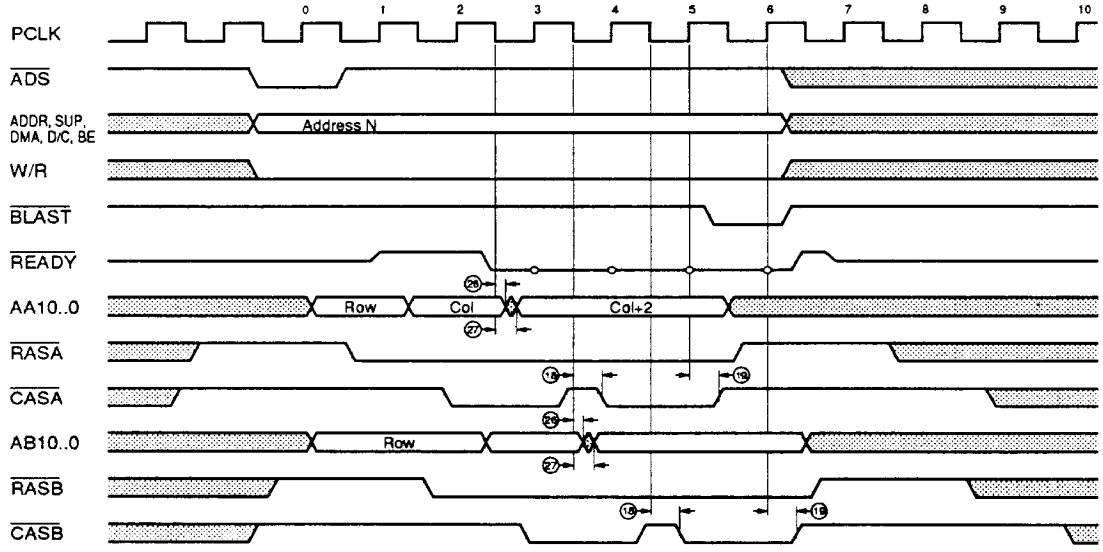


Figure 8 - Burst Access Timing



Functional Overview of Burst Access with Page Compare

Figure 9 diagrams the sequence of events that take place during several typical bursts when the page compare feature is enabled. The sequence begins with a 2 word burst (PCLK 0). Data is ready by PCLK 3 and PCLK 4 (2 wait states for the first access and zero for the second). With the RAS strobes already asserted, the second burst of 4 words can begin after only a single wait state (PCLK 6). The single access that begins with PCLK 11 requires a new row address. Consequently, additional wait states are required since the previous RAS must be terminated and the RAS precharge time of 2 PCLK cycles is inserted.

Table 6 - D.C. Characteristics

#	Symbol	Description	Conditions	Min	Max	Unit
1	V_{IL}	Low Level Input Voltage	V_{CC}=4.75V		0.8	V
2	V_{IH}	High Level Input Voltage	V_{CC}=5.25V	2.0		V
3	I_{IL}	Low Level Input Current	V_{IN}=V_{SS},V_{CC}=5.25V	-10		µA
4	I_{IH}	High Level Input Current	V_{IN}=V_{CC}=5.25V		10	µA
5	V_{OL}	Low Level Output Voltage	V_{IN}=V_{IL} or V_{IH} I_{OL} =24mA		0.4	V
6	V_{OH}	High Level Output Voltage	V_{IN}=V_{IL} or V_{IH} I_{OL}=24mA	3.7		V
7	I_{OZL}	Low Level TRI-STATE Output Current	V_{IN}=V_{IL} or V_{IH} V_O = V_{SS}	-20		µA
8	I_{OZH}	Low Level TRI-STATE Output Current	V_{IN}=V_{IL} or V_{IH} V_O = 5.25V		20	µA
9	I_{CCMax}	Maximum Supply Current Continuous Burst Access	Continuous Simple Access		100 30	mA mA
10	C_{IN}	Input Capacitance			20	pF
11	C_{OUT}	Output Capacitance			20	pF

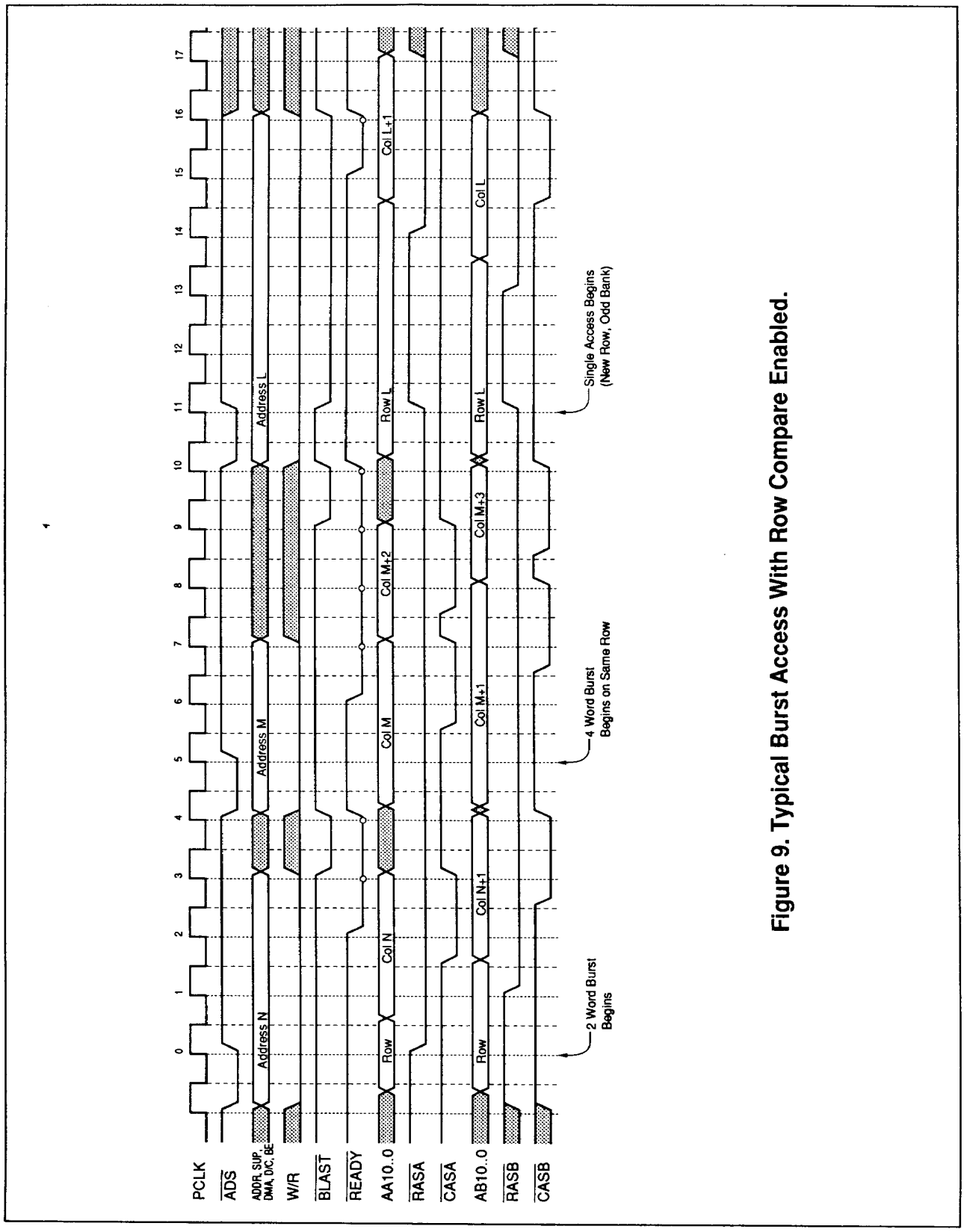


Figure 9. Typical Burst Access With Row Compare Enabled.

Table 7 - Absolute Maximum Ratings

#	Symbol	Parameter	Limits	Units
1	V_{CC}	Supply Voltage	-0.3 to +7	V
2	V_{IN}	Input Voltage	-0.3 to V_{CC}+0.3	V
3	I_{IN}	D.C. Input Current	+/- 50	mA
4	$Ø_{STG}$	Storage Temperature	-65 to 150	°C

All voltages referenced to Ground

Table 8 - Recommended Operating Conditions

#	Symbol	Parameter	Limits	Units
1	V_{CC}	Supply Voltage	4.5 to 5.5	V
2	$Ø_A$	Ambient Temperature Range Plastic Package Ceramic Package	 -0 to +70 -55 to +85	 °C °C

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