SEMICONDUCTOR
THE EMBEDDED CHIPSET COMPANY

***Application Note:***

# Introduction to interfacing the Intel i486™ Processor to the PCI Bus

## *1. Objective*

This application note describes how to interface the ubiquitous Intel i486 microprocessor with the V3 Semiconductor's V962PBC (PBC) PCI bridge and V96BMC (BMC) DRAM controller. Target applications include PCI based adapter cards and i486 based embedded systems.

Throughout this document, references will be made to the operation of the V962PBC and V96BMC components. Basic familiarity with these devices is assumed. If you don't have the relevant data sheets and user manuals for them then please contact V3.

You can also download them from the V3 Semiconductor WEB site at:

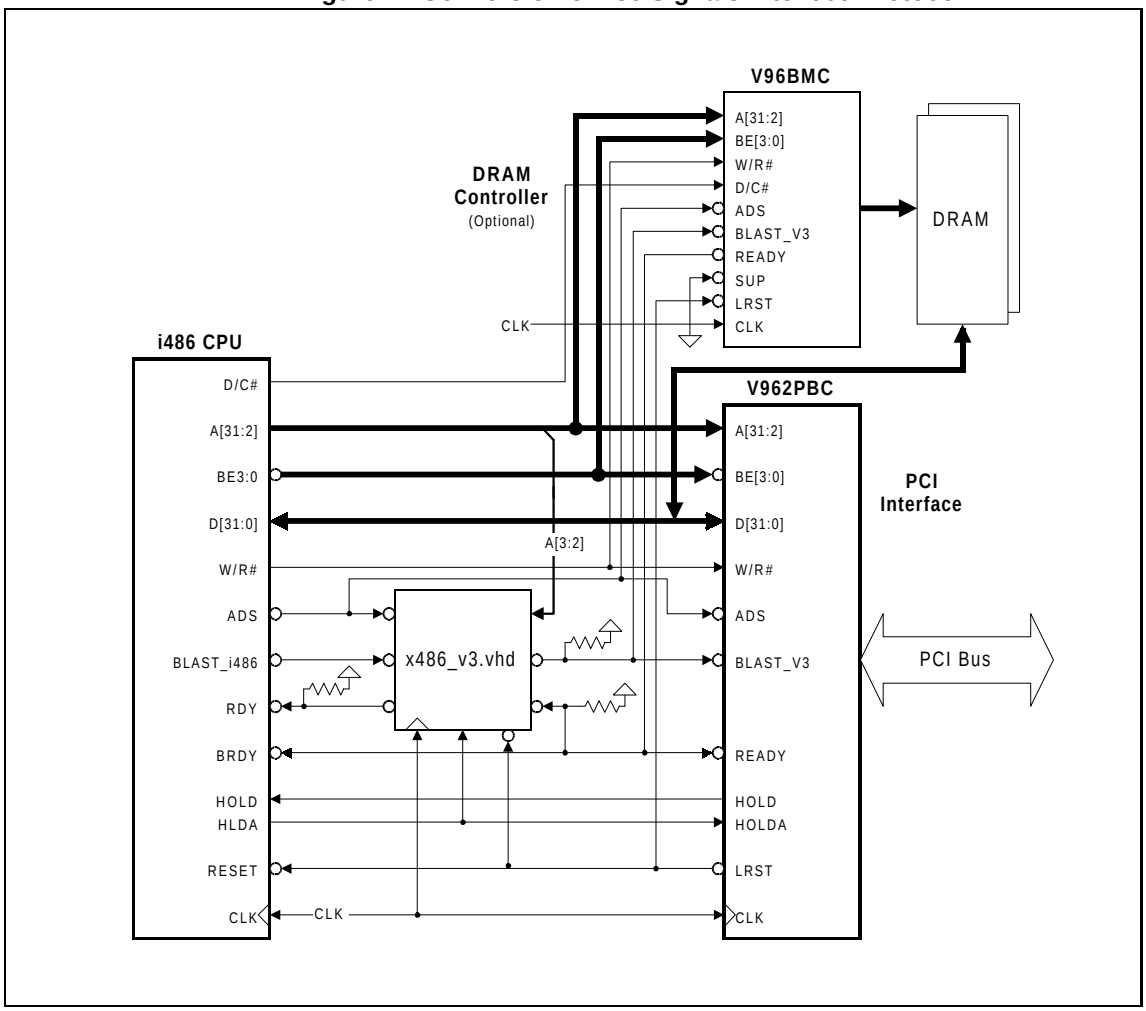
http://www.vcubed.com.

## *2. Overview*

Although the V962PBC and V96BMC are designed to interface gluelessly to the Intel i960Cx processor, the interface adapts equally well to the i486. The main difference between the two bus protocols is that the i486 performs a toggle burst while the i960 always performs a linear burst. Fortunately, the i486 provides a method of terminating a burst early. This feature is used in this application note to convert non linear bursts from the 486 into linear bursts for the V962PBC and V96BMC.

# 3. Interconnection

**Figure 1: Conversion of 486 Signals into i960 Protocol**



# 4. PLD Design

To obtain detailed design information and PLD source code, please contact V3 Semiconductor at:

EMAIL: v3help@vcubed.com

URL: http://www.v3semiconductor.com/

Applications Engineering: (416) 497-8884

Sales and Marketing: 1-800-488-8410 or (408) 988-1050

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# 5. Performance

The performance of the various alternatives have been calculated in the following tables (TBD). "Real world" performance will depend on a number of factors:

- Bursting
- Data flow
- Sequential Reads
- System Bottlenecks

# 6. Conclusion

The V962PBC from V3 provides a high performance PCI solution for various members of the Intel processor family. When used together with the V96BMC burst DRAM controller, the limited burst capabilities of the i486 are addressed satisfactorily. Only a small (44 pin) low cost (< $2) PLD is required in addition to the highly integrated V962PBC and optional V96BMC.